

FOXCONN CONFIDENTIAL
DO NOT DISTRIBUTE

Lenovo G41R

commercial mATX

Project Information

Phase: SVT Ver:1.0 2009/08/07
BOM: LENOVO-G41R-UATX-LC_EZBOM_
SVT_0[1].6_111009
SVID: 17AA
SSID: 301B

BIOS Licence Label

LBL2
BIOS_LICENCE
Note:
AMI Legacy

PCB Fab Note

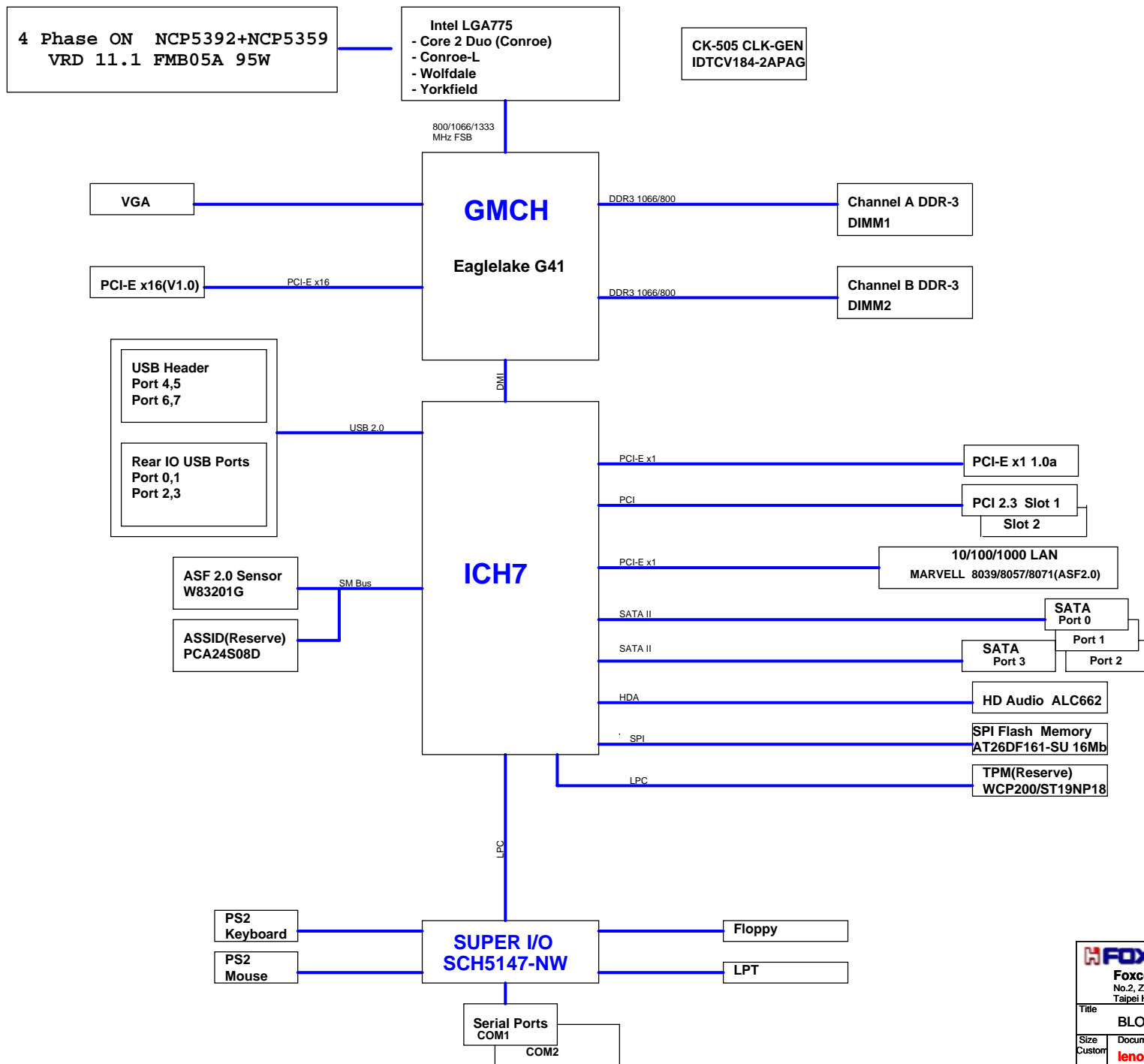
PCB1
Printed Circuit Board
PC BOARD
CRITICAL
4-Layer PCB,Color With GREEN Soldermask,White Silkscreen,9.6X9.6 inch,Double Side OSP,Rev:1.0,ROHS
010133F00-574-G

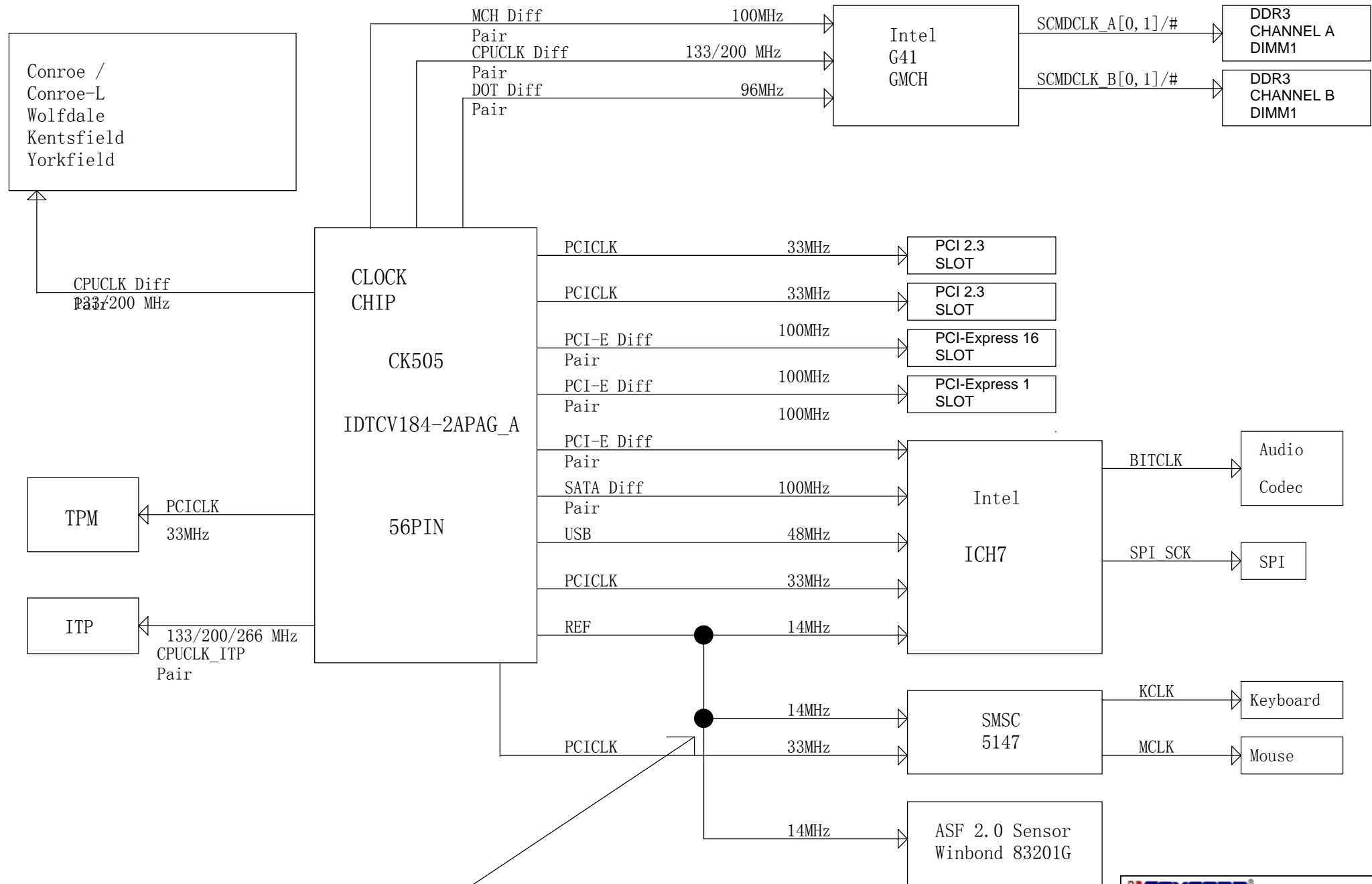
DESCRIPTION	COPPER(Oz)	THICKNESS(MILS)
A-TOP SIGNAL LAYER	5(BEFORE PLATING)	1.9(+0.8/-0.8)
B (P.P 1080)		2.7(+0.8/-0.4)
C-POWER LAYER	1	1.2(+/-10%)
D		47(REF)-OPEN
E-GROUND LAYER	1	1.2(+/-10%)
F(P.P 1080)		2.7(+0.8/-0.4)
G-BOTTOM SIGNAL LAYER	5(BEFORE PLATING)	1.9(+0.8/-0.8)
TOTAL		59MILS(+8MILS,-5MILS)

PAGE	TITLE
01	TOC/SCH Changes
02	Block Diagram
03	Clocks Diagram
04	Power Distribution
05	Power Flow
06	Power Good Diagram
07	Power Sequence Diagram
08	Reset Diagram
09	Clock Generator - CK505
10	TPM and Assert ID
11	ASFSen,,Assert ID,CaseOpen
12	P4-LGA775 Signals 1
13	P4-LGA775 Signals 2
14	P4-LGA775 Power 1
15	XDP Conn./DMI debug header
16	MCH-CPU FSB Interface
17	MCH-DDR3 Memory Channel A
18	MCH-DDR3 Memory Channel B
19	MCH-PCI-E x16/Graphics.
20	MCH-VGA/MISC
21	MCH-Power/GND
22	MCH-Power Decoupling/Filter
23	Chipset Sequencing
24	ICH7 1
25	ICH7 2
26	ICH7 3-4
27	DDR3 CH-A DIMM1
28	DDR3 CH-B DIMM1
29	USB Power
30	USB 2.0 Connector
31	Audio Codec Realtek ALC662
32	Audio Front/Rear Connector
33	SATA and FDD
34	PCI Slot1
35	PCI Slot2
36	PCIE x1 Slot
37	PCIE x16 Slot
38	SuperIO SMSC5147
39	Parallel / Serial Ports
40	PS2_KBD-Mouse
41	VGA Port
42	SPI EEPROM
43	Power Input/ EMI CAP/MINT
44	Front Conn./LED/FRISW
45	Chassis / CPU / PSU Fan HD

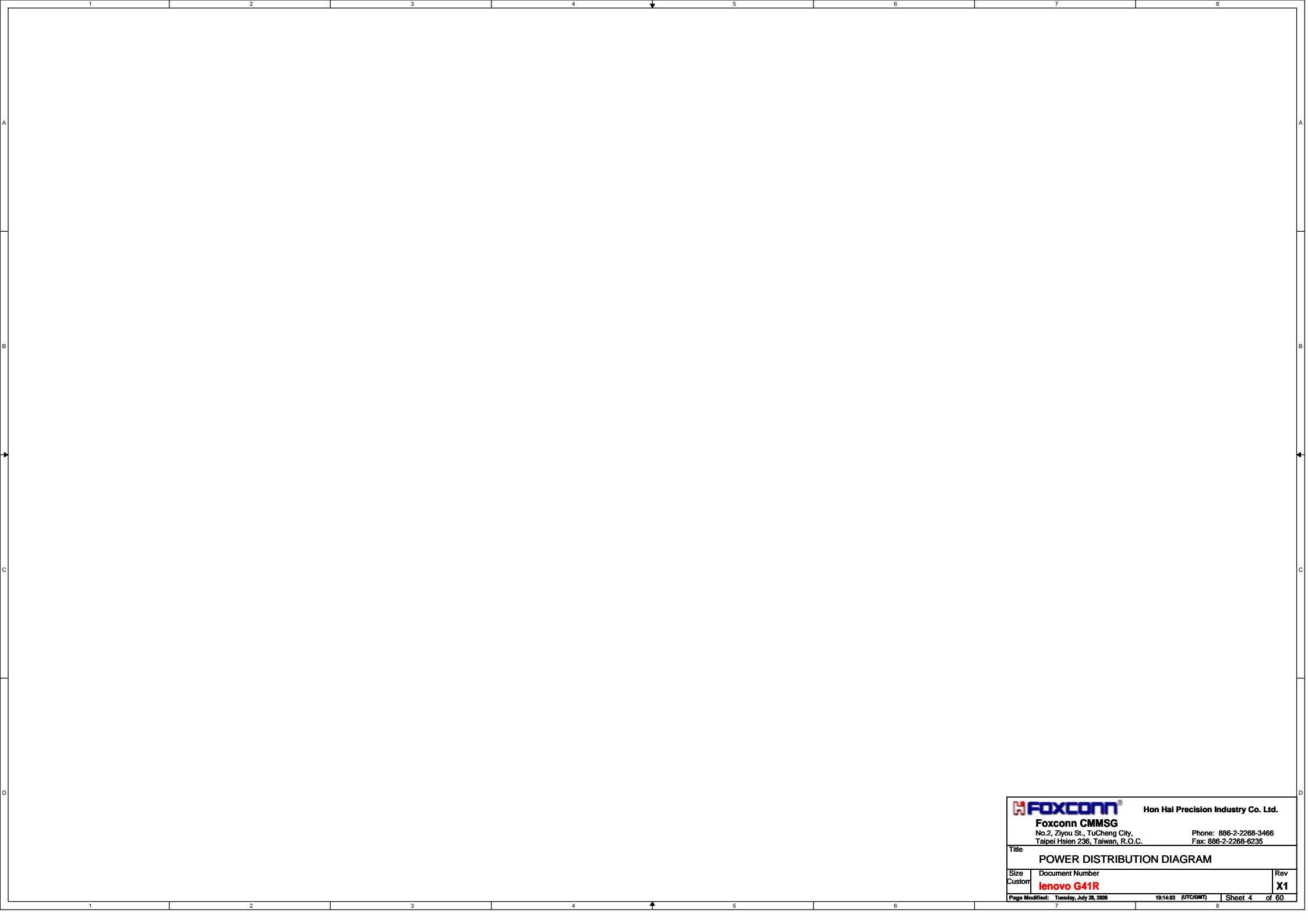
46	MARVELL 88E8057
47	LAN Power
48	RJ45
49	LPT_PS2 header
50	+VCORE Controller
51	+VCORE Phase1 & Phase2
52	+VCORE Phase3 & Phase4
53	+5V_Dual & +5V_Dual_USB_B
54	+3P3VSB
55	+1P5V_DUAL & +VTT_DDR
56	+1P1V
57	+1P2V_FSB_VTT & +1P5V
58	ICH GPIO Information
59	BIOS Routing Information
60	Change list


BLOCK DIAGRAM

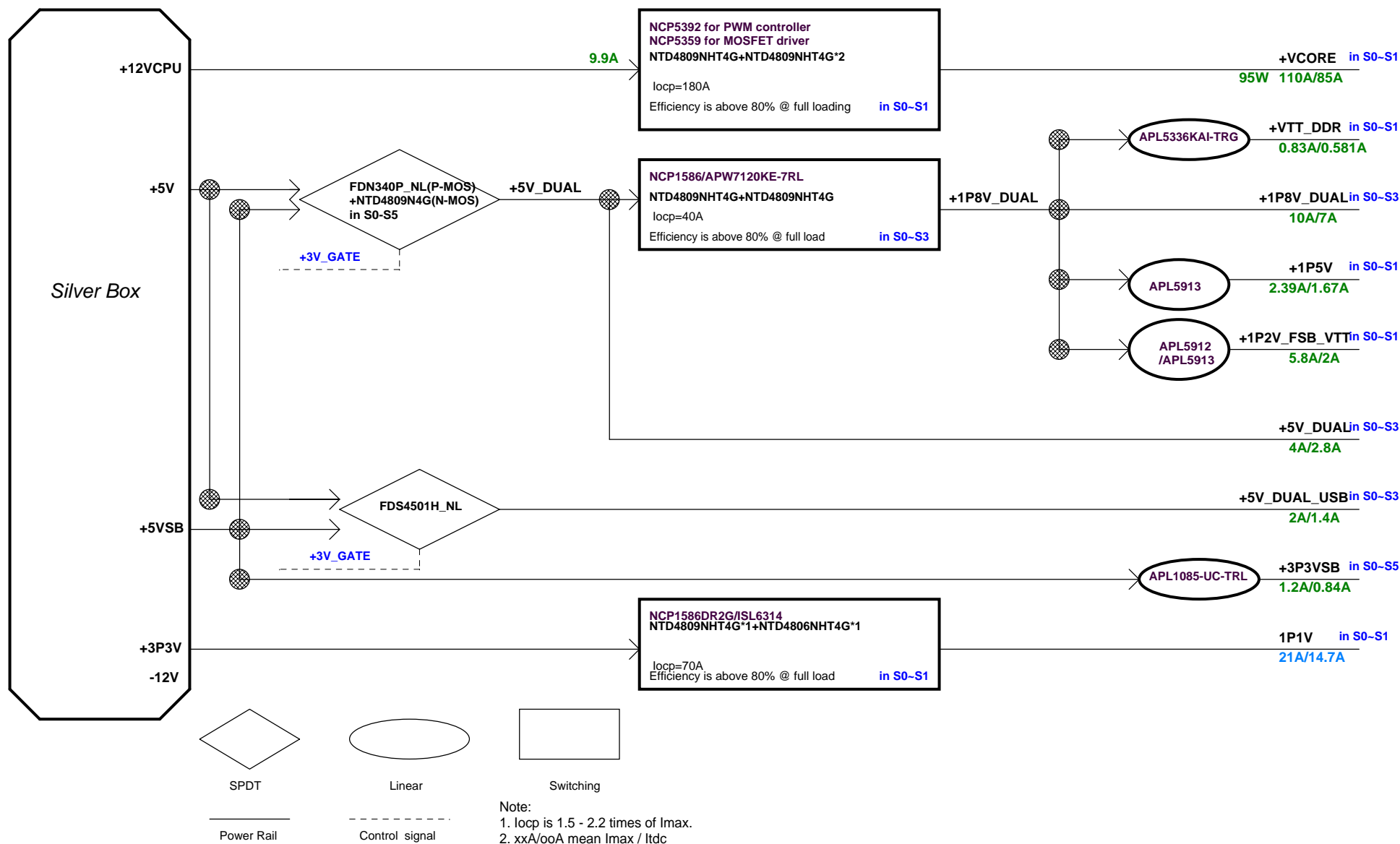


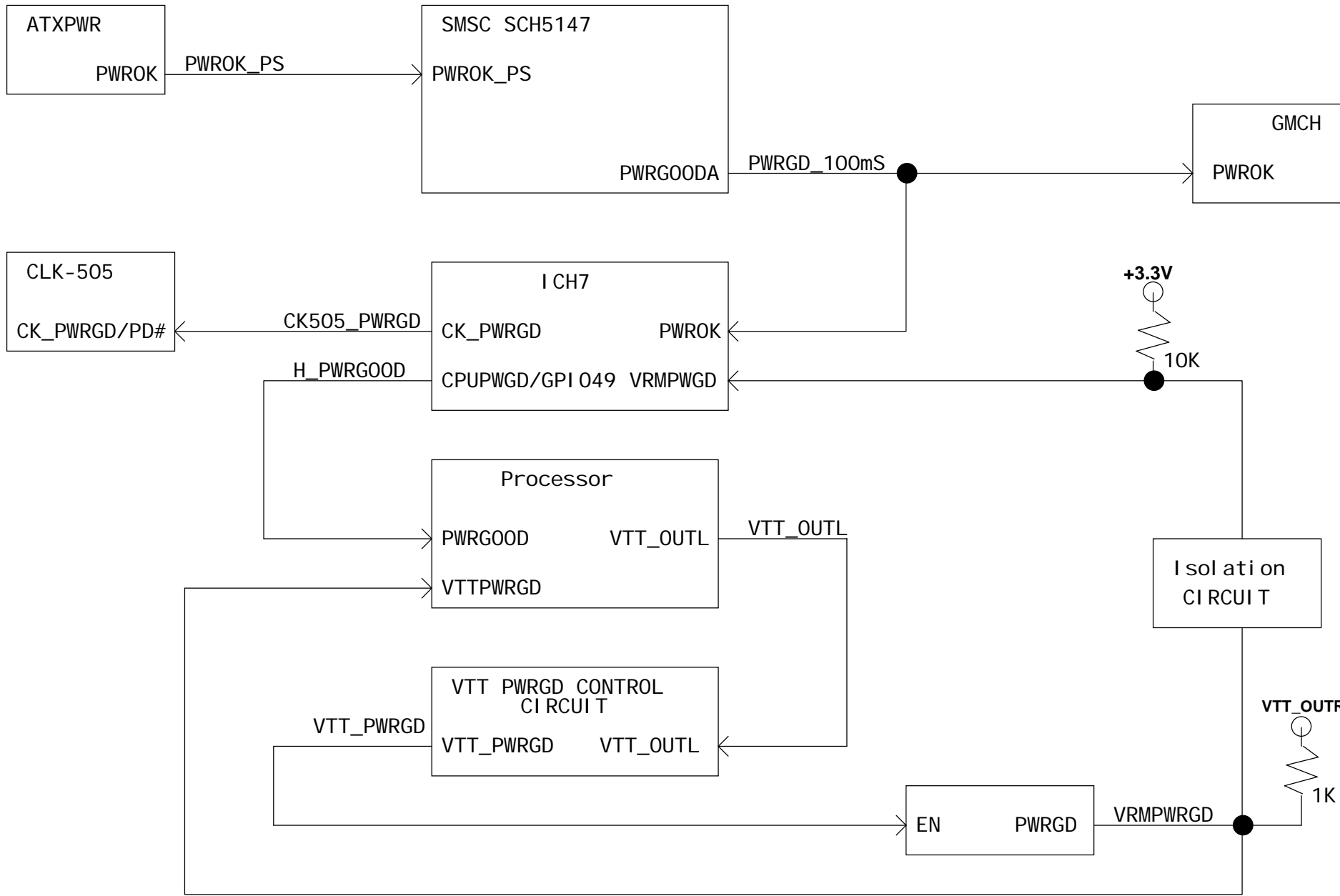


One Source Driver 3 device
High Risk

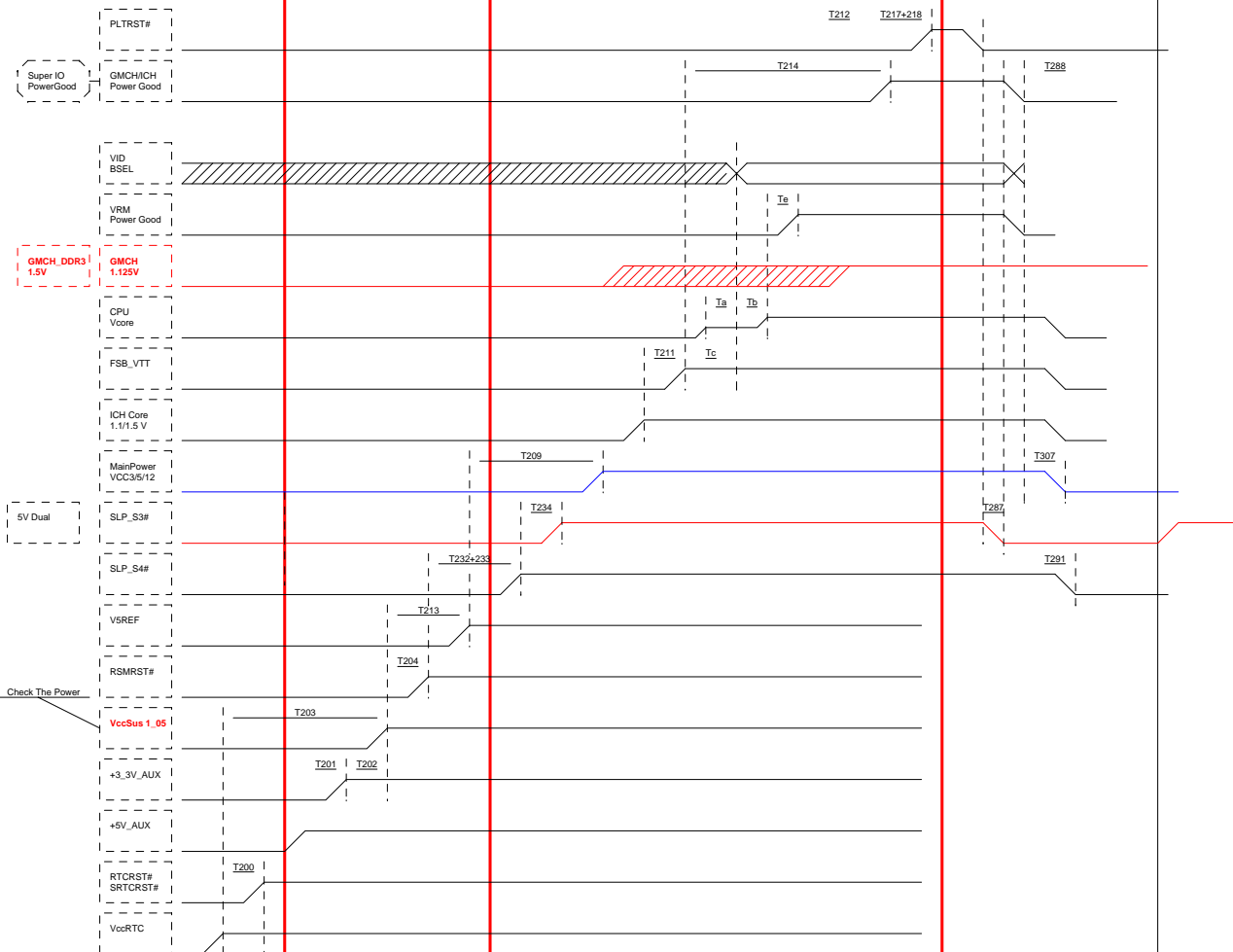


		Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG			
No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.		Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
Title			
POWER DISTRIBUTION DIAGRAM			
Size	Document Number		Rev
Custom	lenovo G41R		X1
Page Modified: Tuesday, July 28, 2009		16:14:03 (UTC+8)	Sheet 4 of 60





Power Sequence Diagram

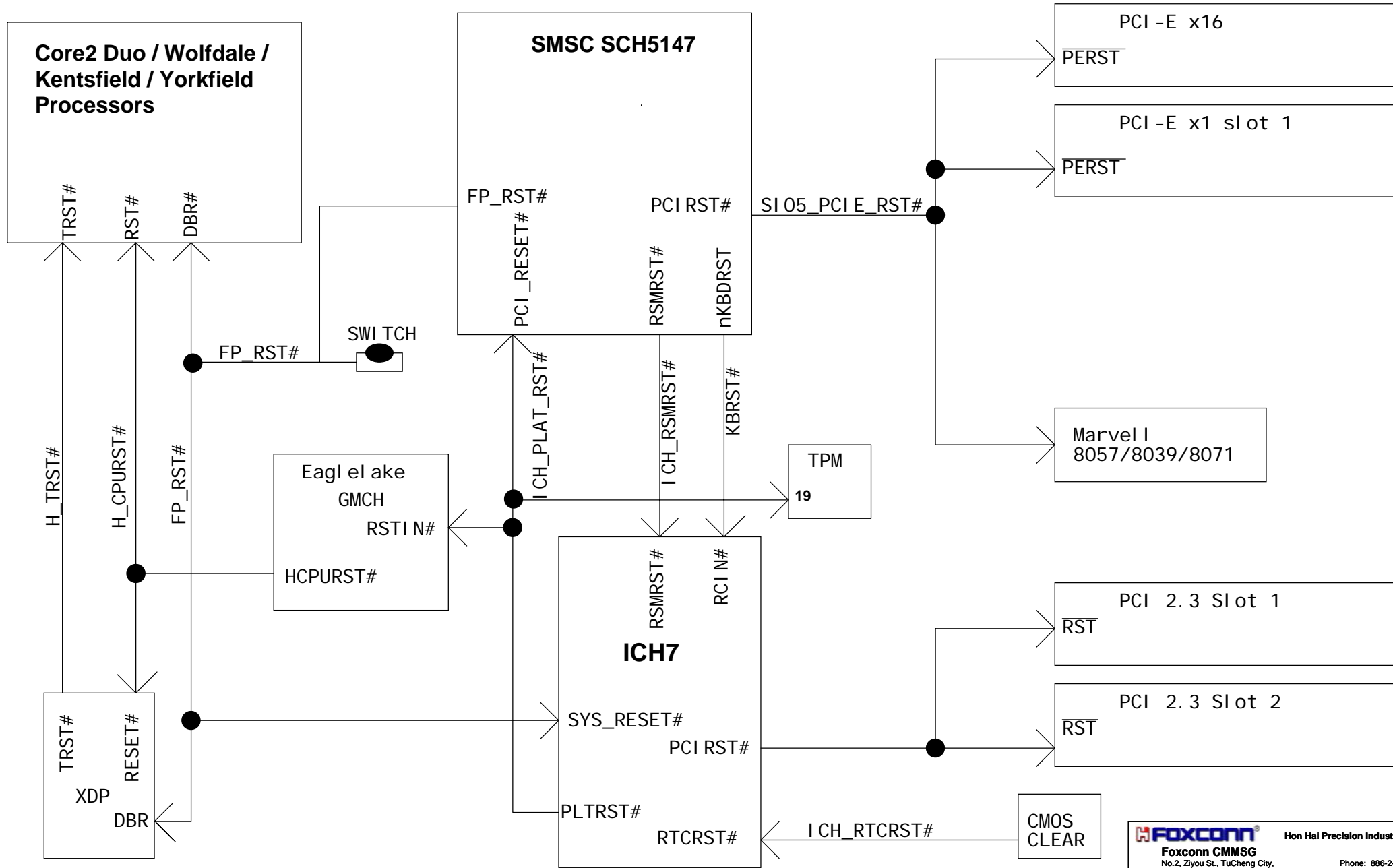


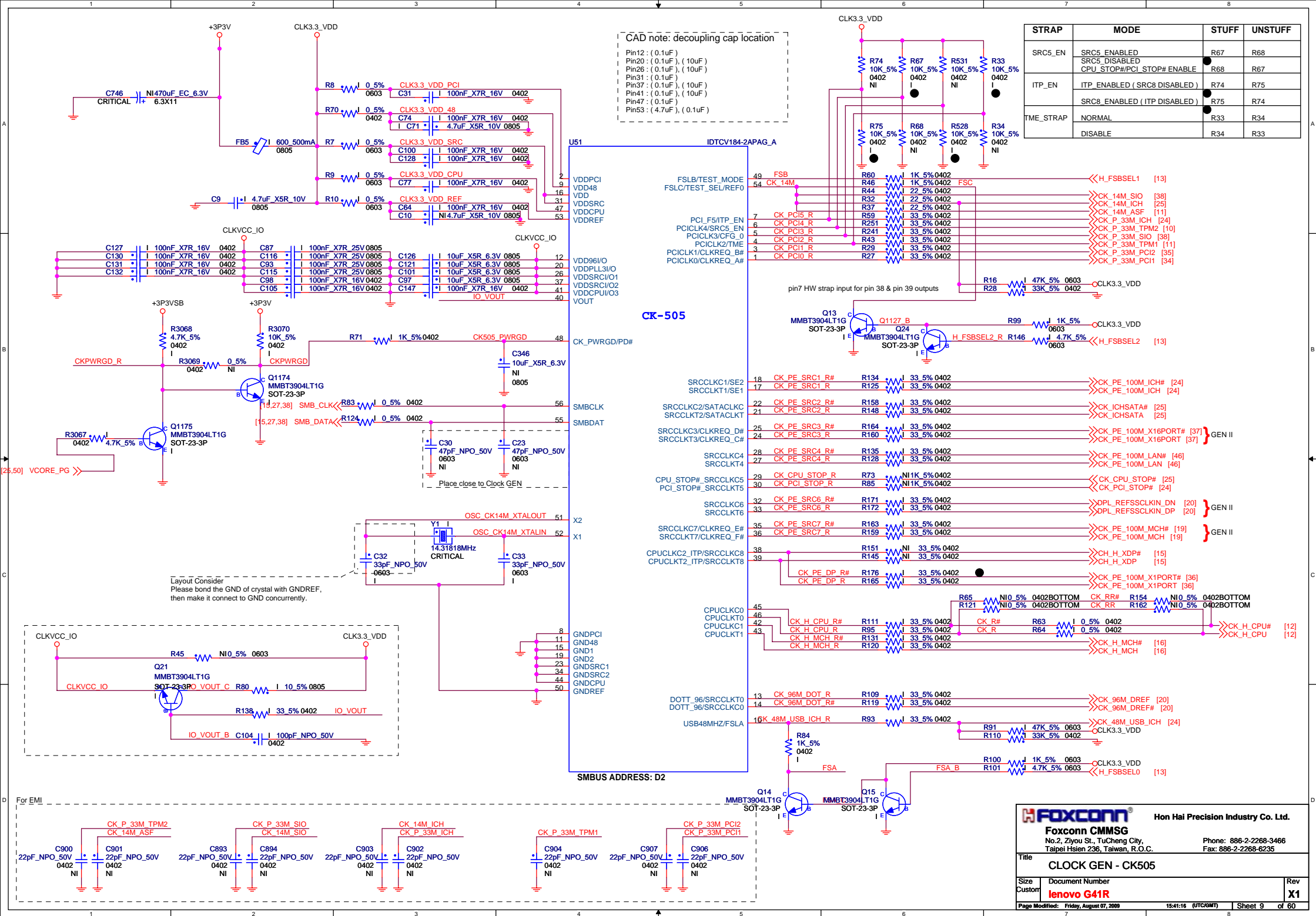
	Parameter	Min	Max	Units
Ta(T43)	VCC_BOOT stable to VID/BSEL valid	-10	xx	μs
Tb(T44)	VID/BSEL valid to Vcc stable	-100	xx	μs
Tc(T45)	VTT stable to VID/BSEL valid	-10	xx	μs
td(T41)	VCC stable to PWRGOOD assertion	0.05	500	ms
T209	V5REF active to Vcc3_3 active	0	xx	ms
T211	Vcc1_5 active to V_CPU_IO active	Notes 4	xx	ms
T212	VMPWRGD active to PWRGD active	5	xx	ms
T213	VccSus supplies active to Vcc supplies active	0	xx	ms
T214	Vcc supplies active to PWRGD	95	xx	ms
T201	V5REF_Sus active to VccSus3_3 active	0	xx	ms
T202	VccSus3_3 active to VccSus1_1 active	Notes 2	xx	ms
T203	VccRTC supply active to VccSus supply active	0	xx	ms
T204	VccSus supplies active to LAN_RST# inactive, RSMRST# inactive	0	xx	ms

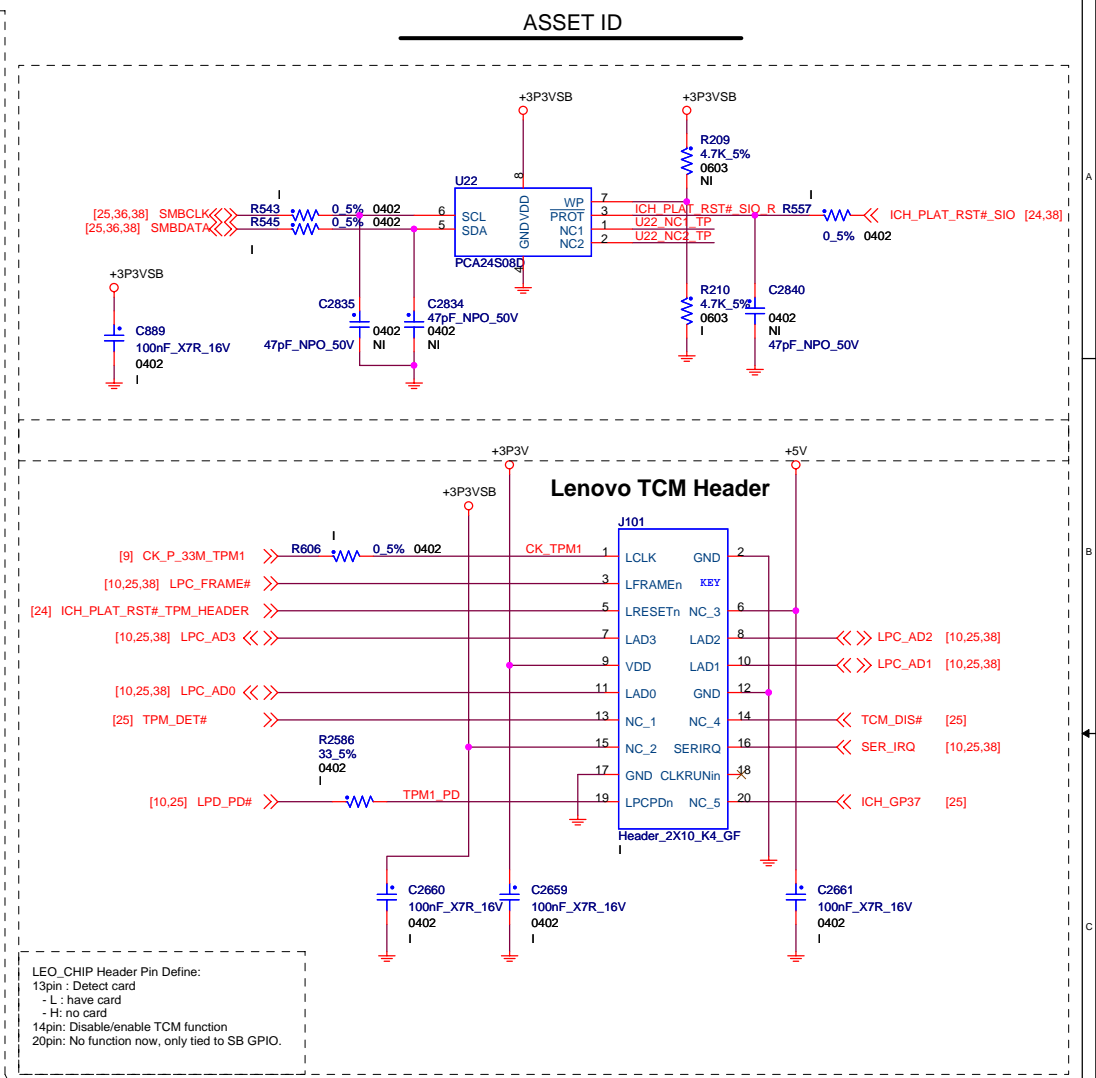
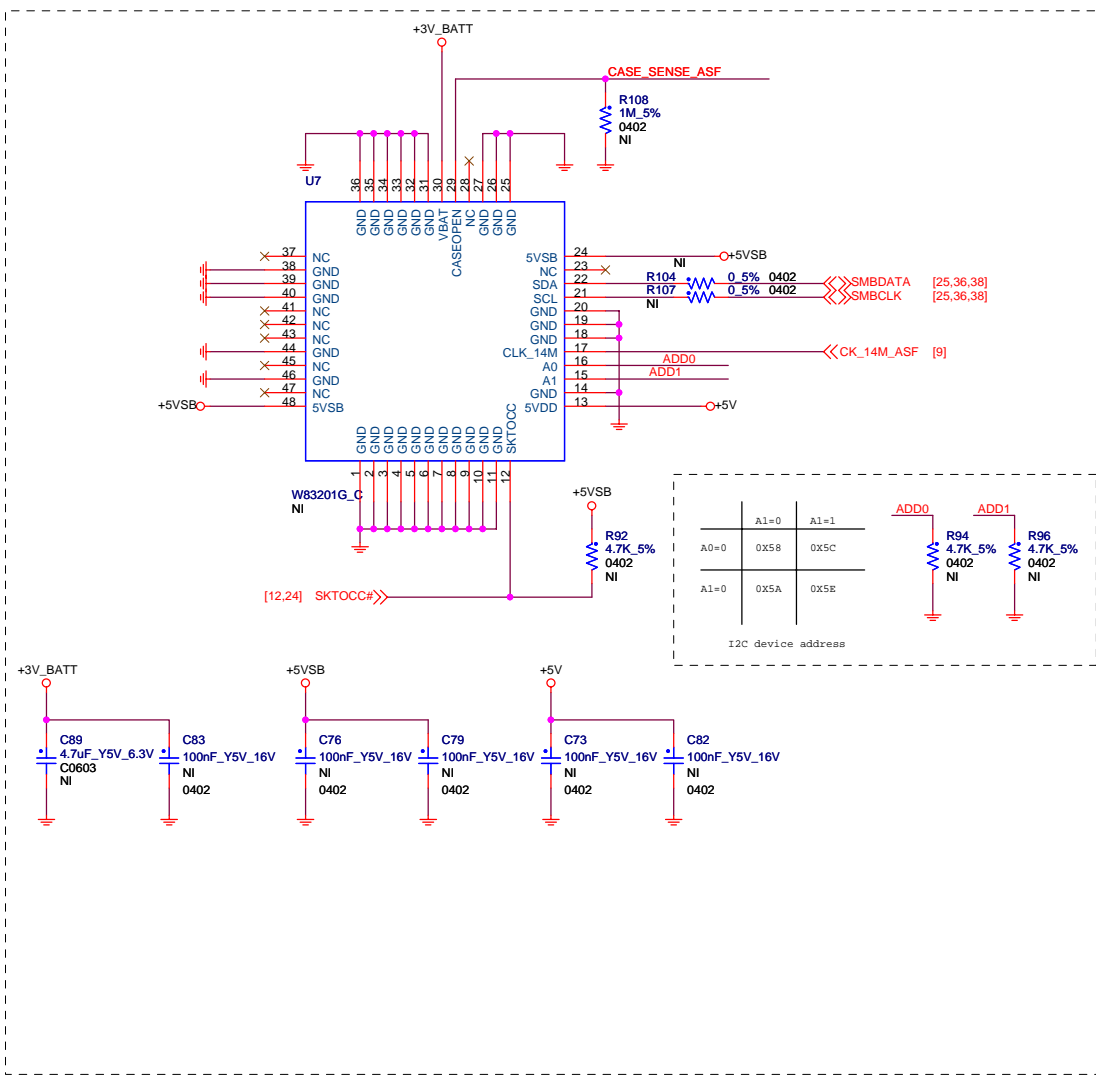
Notes

- The associated 3.3 V and 1.05 V supplies are assumed to power up or down "together".
- Vcc1_5 must power up before V_CPU_IO or after V_CPU_IO within 0.7 V. b) V_CPU_IO must power down before Vcc1_5 or after Vcc1_5 within 0.7 V.

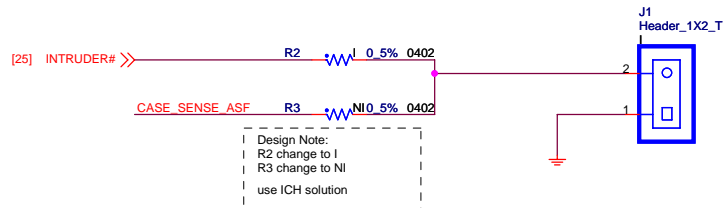
T204	PWRGD, VMPWRGD inactive to Vcc supplies inactive (nominal voltage -5%)	Min 20	ns
------	--	-----------	----



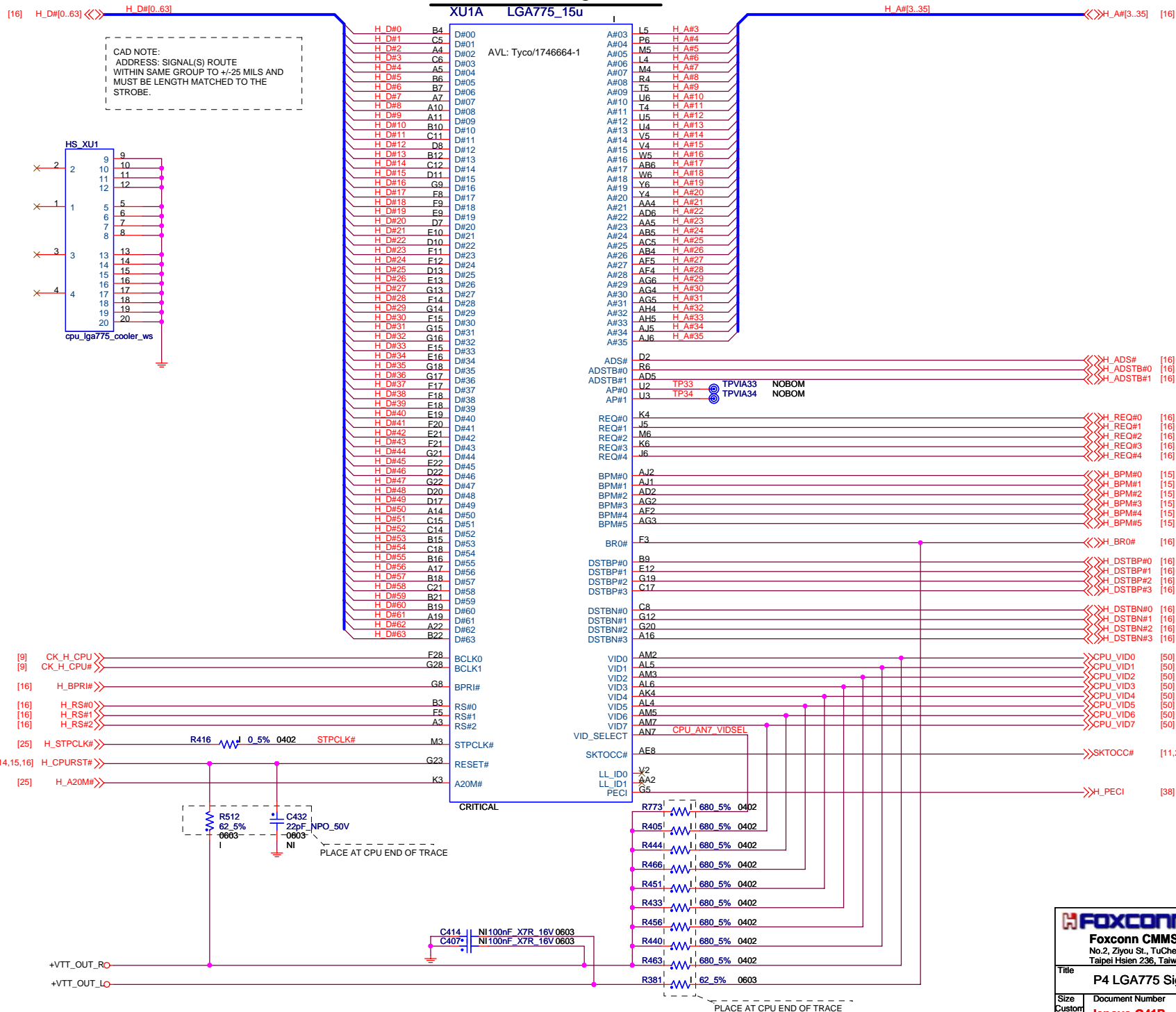




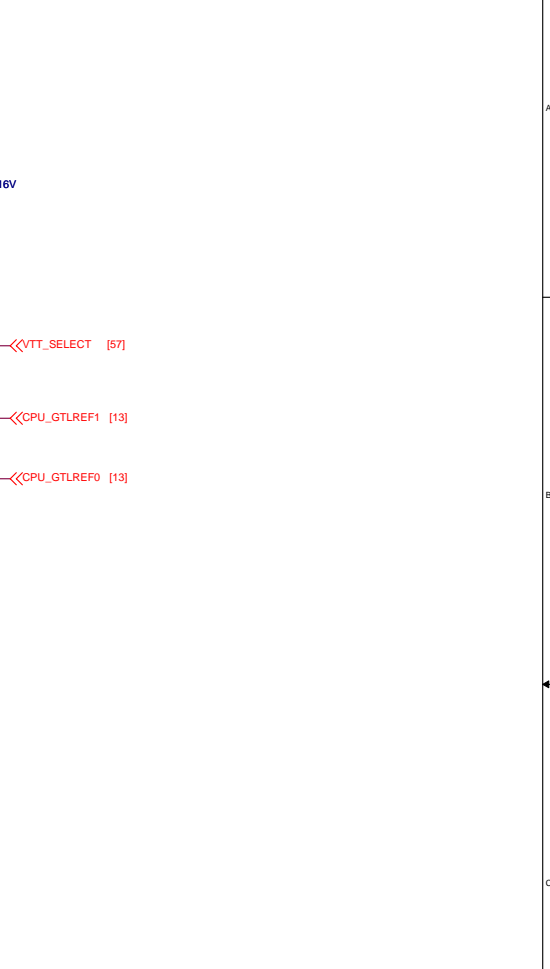
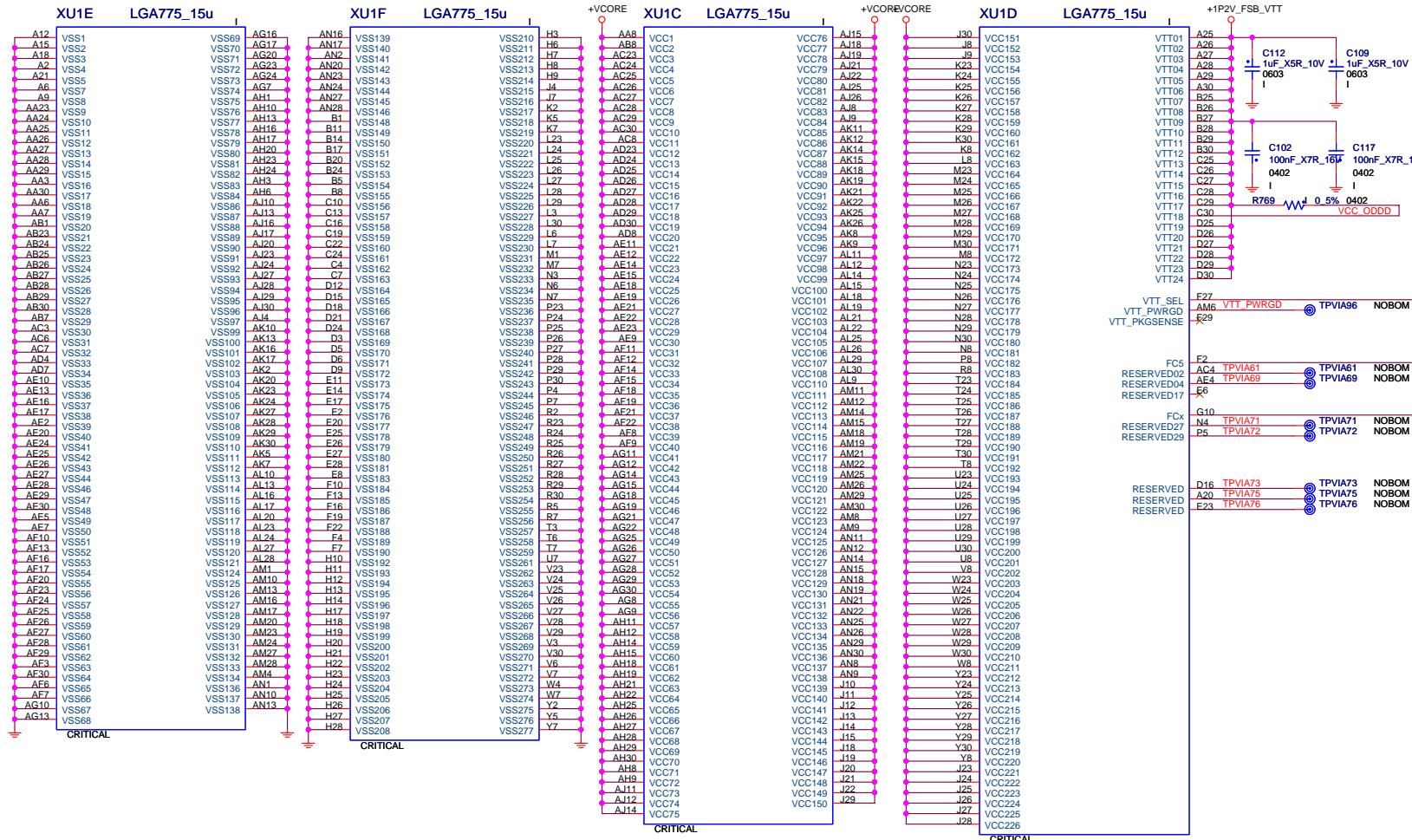
Lenovo Case Open
 Special Material need to check AND make sure Pin1.



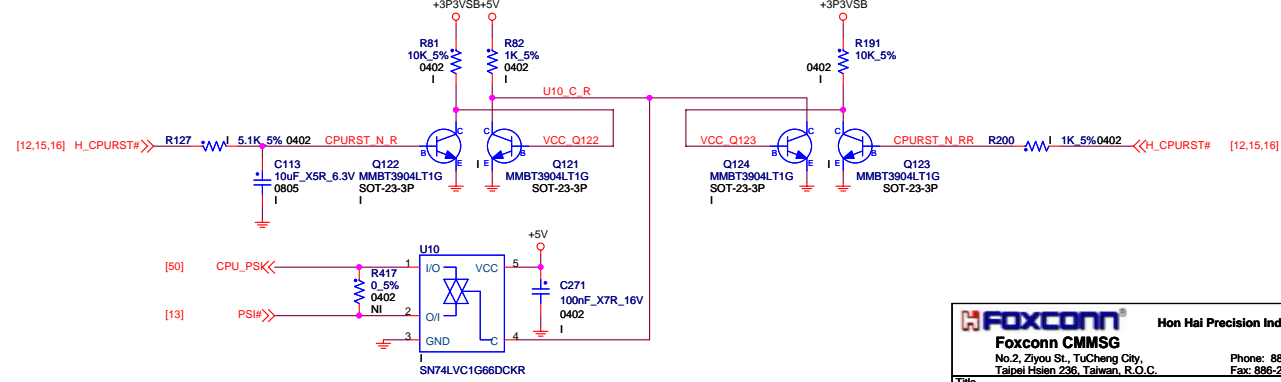
P4 LGA775 Signals 1



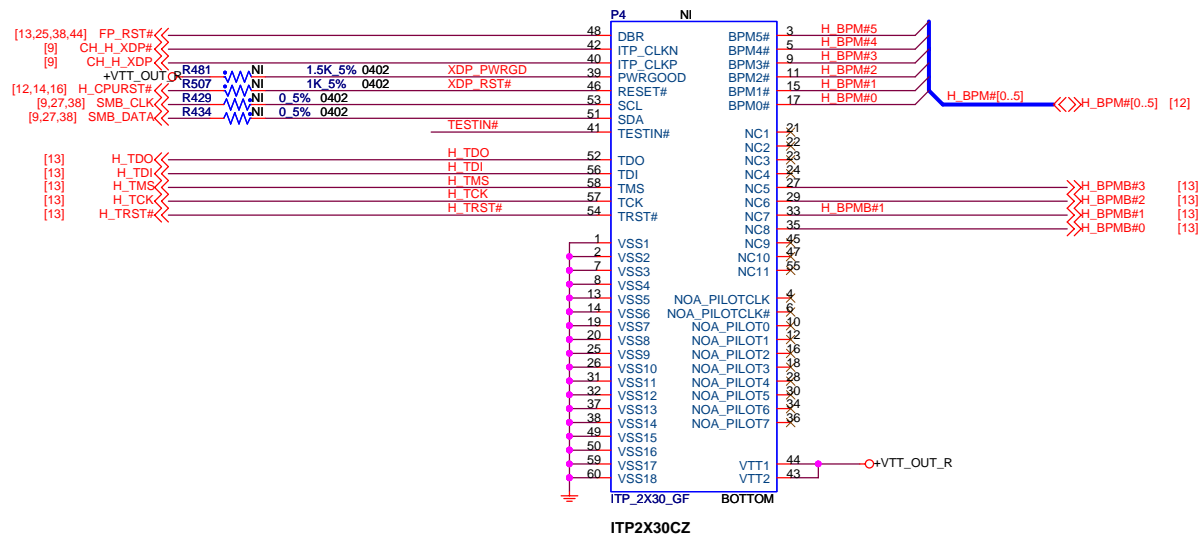
P4 LGA775 Power



Design Note:
C-step Erratum for PSI
Wellfare and Yorkfield processors have a C-step erratum for PSI
The PSIF signal will improperly be asserted during power-on
The assertion will occur while the processor RESET# is asserted
The assertion will extend beyond RESET# signal deassertion for a short duration
After completing power-on, the PSIF signal will not assert for C-step
E-step has a planned fix for this erratum
Intel designed, and will validate, a circuit to work around this erratum
The circuit blocks the errant PSIF signal assertion, only allowing the PSIF signal to pass to the VR after ~50ms after RESET# is deasserted (see later slide)
Objective was to enable a circuit to allow for a single Eaglelake board BOM that is compatible with C-step (without PSI support) and E-step (with PSI support)

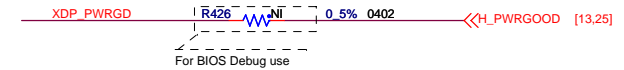


Intel XDP Debugging Connector

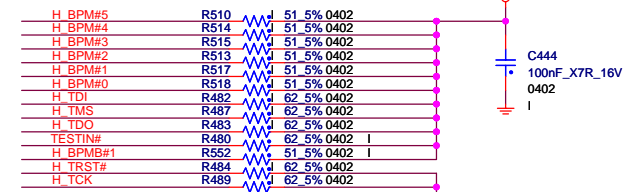


XTP CAD NOTES:

- Place XP port 2 to 4 inches from processor in solder side.
- Match Impedance of the BPM signals to 50 ohm and trace width to 5 mils with 10 mil spacing.
- TCK signal spacing should be 5 mil trace and 10 mil spacing. TCK should split at the XTP and route to CPU.
- FBO signal spacing should be 5 mil trace and 10 mil spacing. Match FBO length to the length of BPM segment from XTP to CPU.
- TMS# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain with pull-up at XTP port.
- TRST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain startinf from XTP to CPU.
- CPU_RST# signal spacing should be 5 mil trace and 10 mil spacing. Route in daisy chain starting from GMCH to CPU.
- TDI,TDO signal spacing should be 5 mil trace and 10 mil spacing.
- Other signals should have 5 mil trace and 10 mil spacing.



W=4, S=5 mil Processor to XDP <1.5", a branch to Rpu <1.0".
PLACE BPM TERMINATION NEAR CONNECTOR.



CPU XDP TERMINATION.

BPM#[0..5] : the length accounts for both the distance from the CPU to XDP connector and the sub to the termination should less than 1.5".

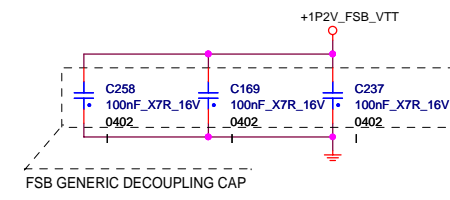
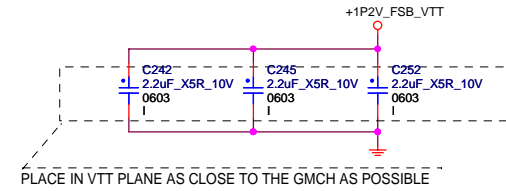
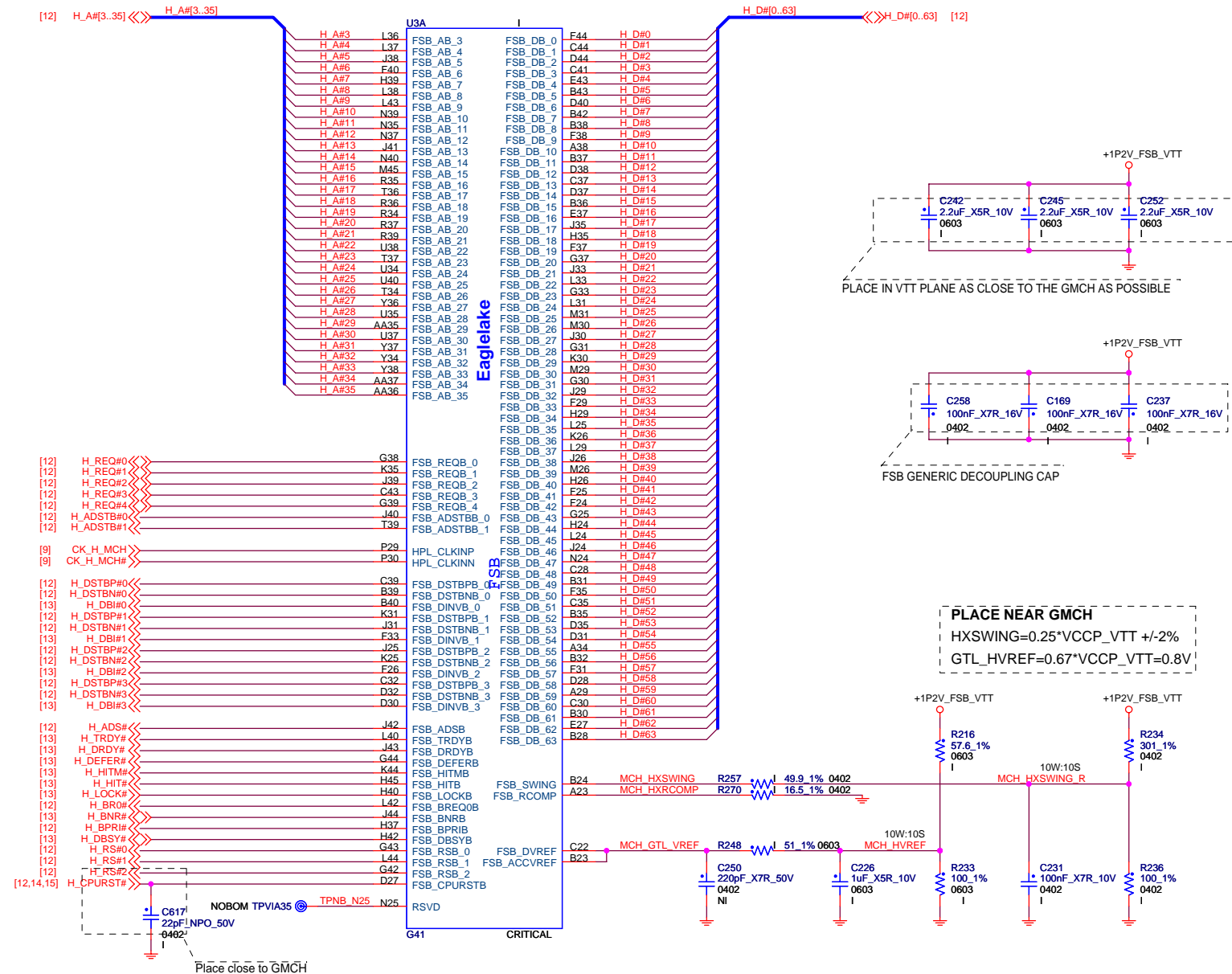
PLACE TMS/TDI TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TDO TERMINATION NEAR CONNECTOR.

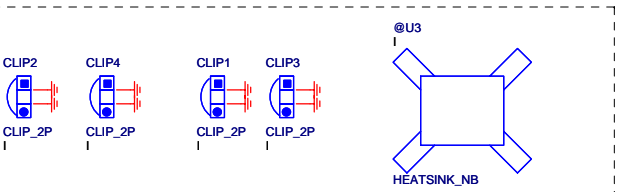
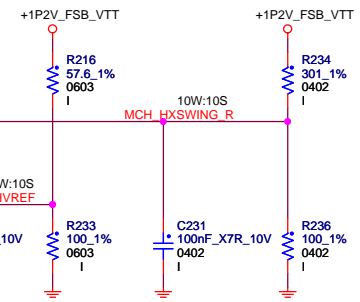
PLACE TCK TERMINATION NEAR CPU WITHIN 1.5" OF CPU.

PLACE TRST# TERMINATION ANYWHERE ON ROUTE.

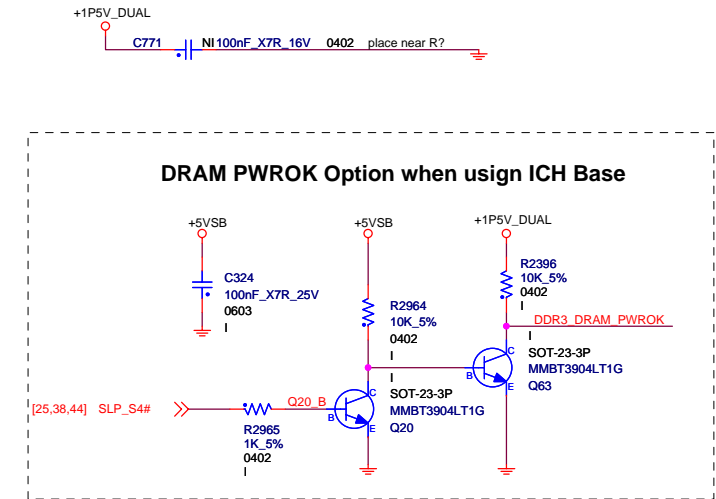
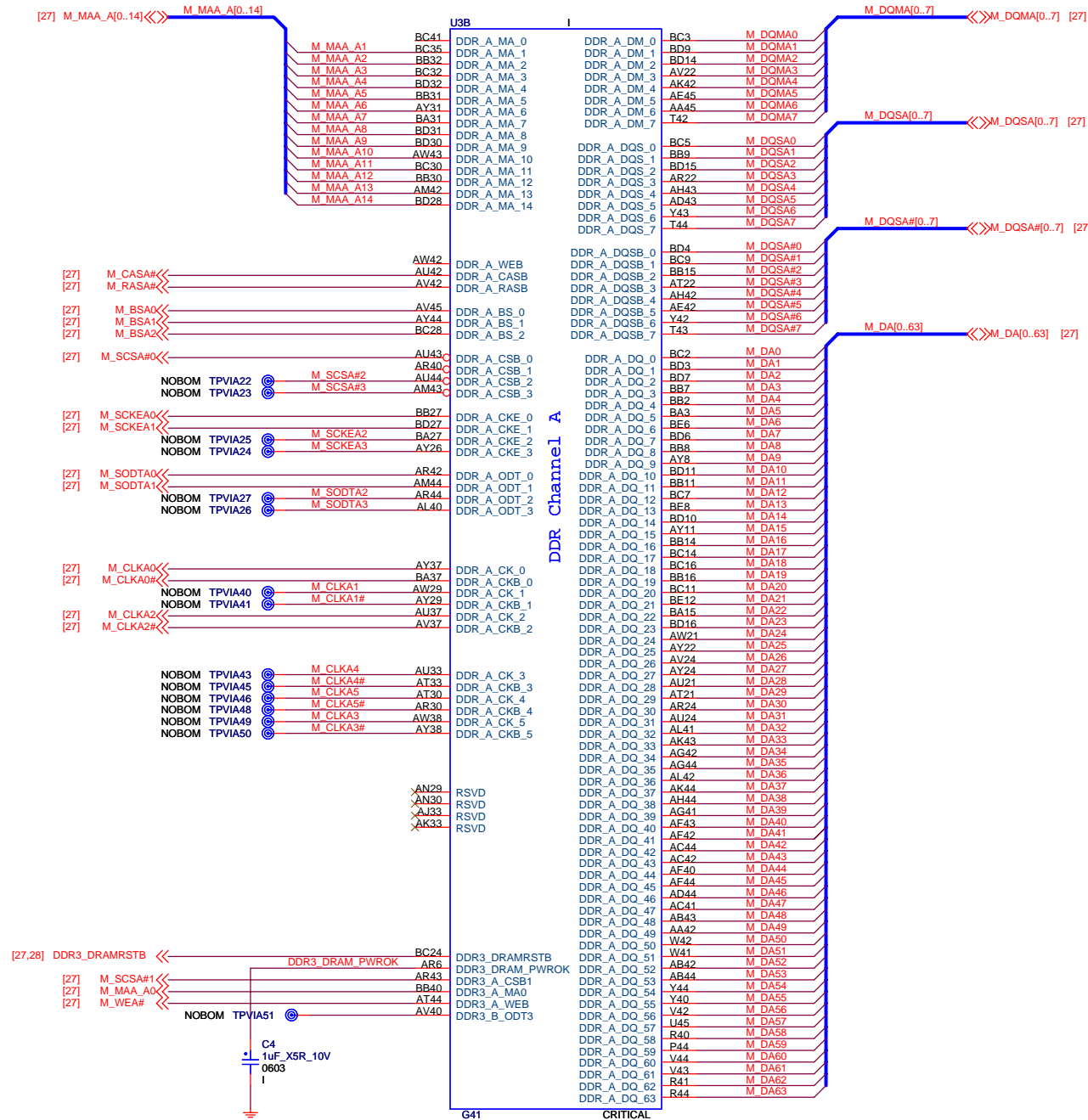
MCH-CPU FSB Interface



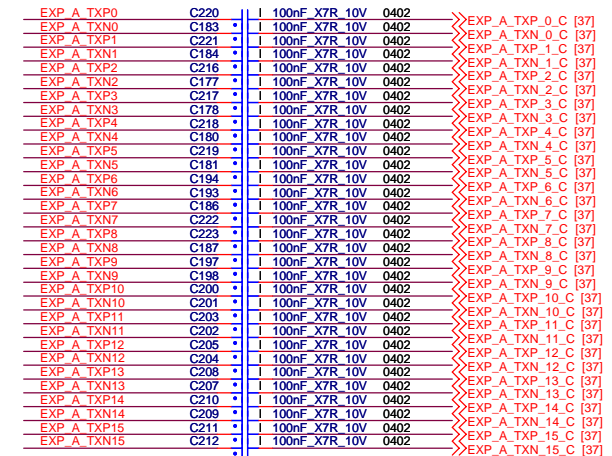
PLACE NEAR GMCH
HXSWING=0.25*VCCP_VTT +/-2%
GTL_HVREF=0.67*VCCP_VTT=0.8V



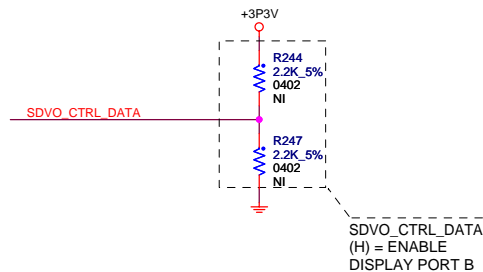
MCH-DDR3 Memory Channel A



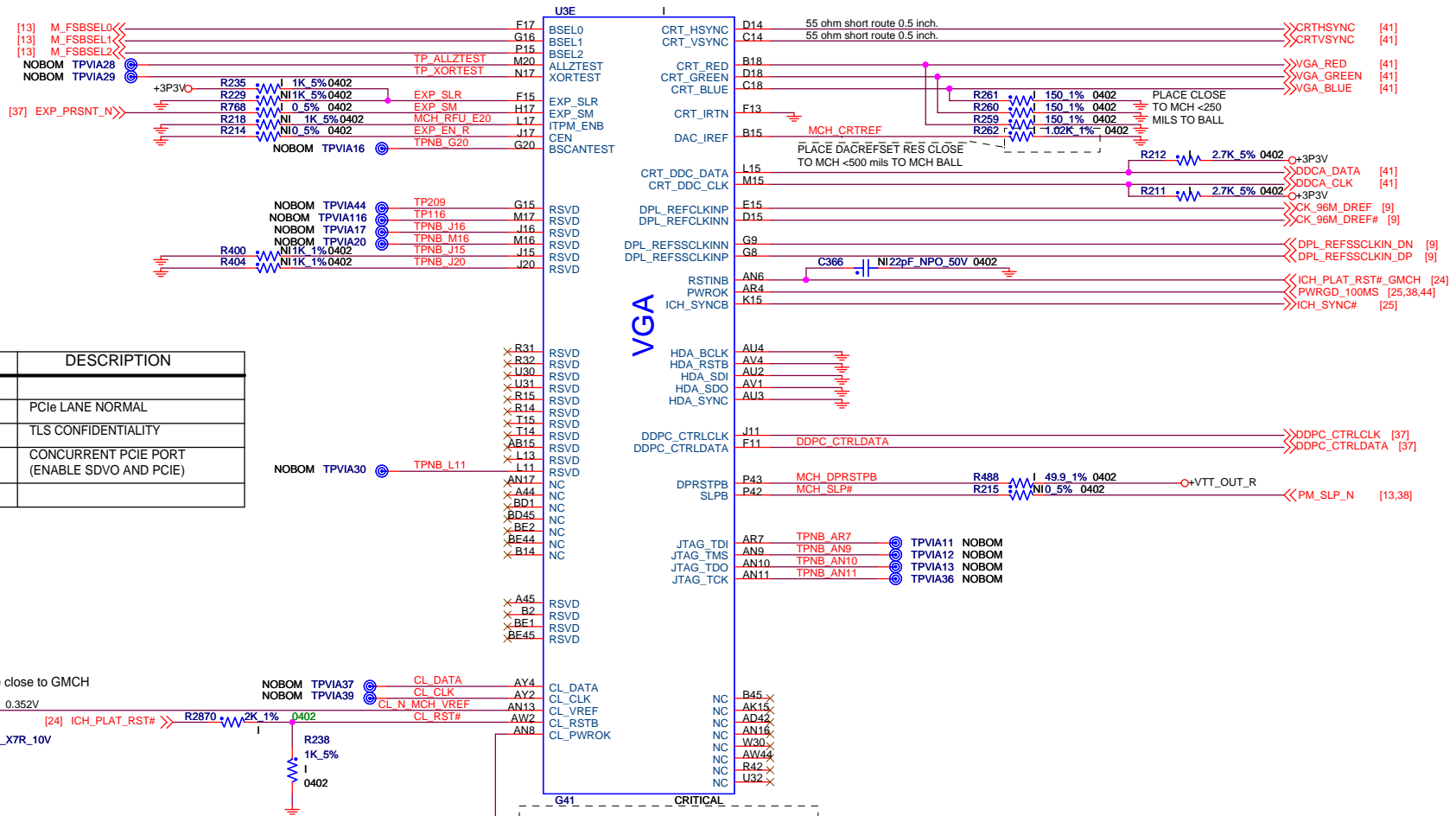
AC coupling caps must be placed within .250" of PCI x16 Graphics connector



	H	L	DESCRIPTION
MCH_MTYPE	NOT IN PRIMARY SLOT	PRIMARY SLOT	PRIMARY_PEG_PRESENCE
DUALX8 ENABLE	1X16 PCIE PORT ENABLE	2X8 PCIE PORT ENABLE	PCIE PORT BIFURCATION

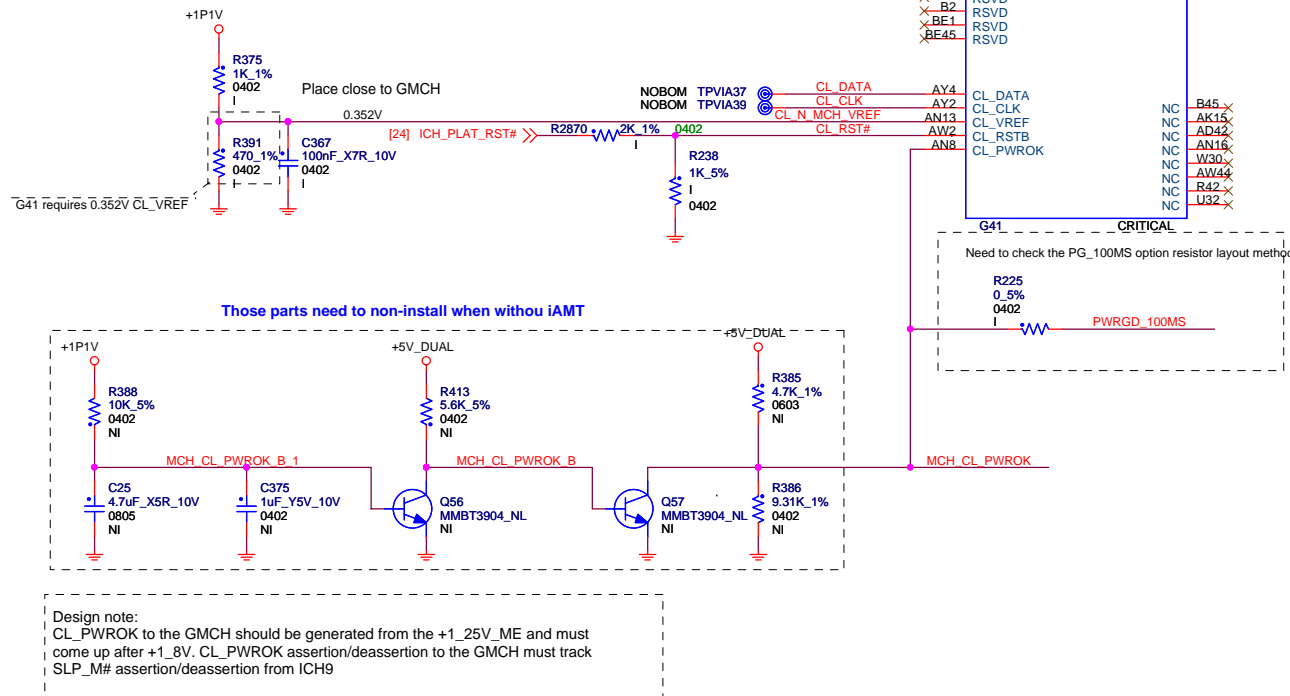


MCH-VGA/MISC



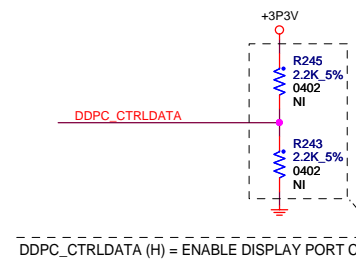
BSEL TABLE			
2	1	0	FSB FREQUENCY
0	0	0	266 MHZ (1067)
1	0	0	333 MHZ (1333)

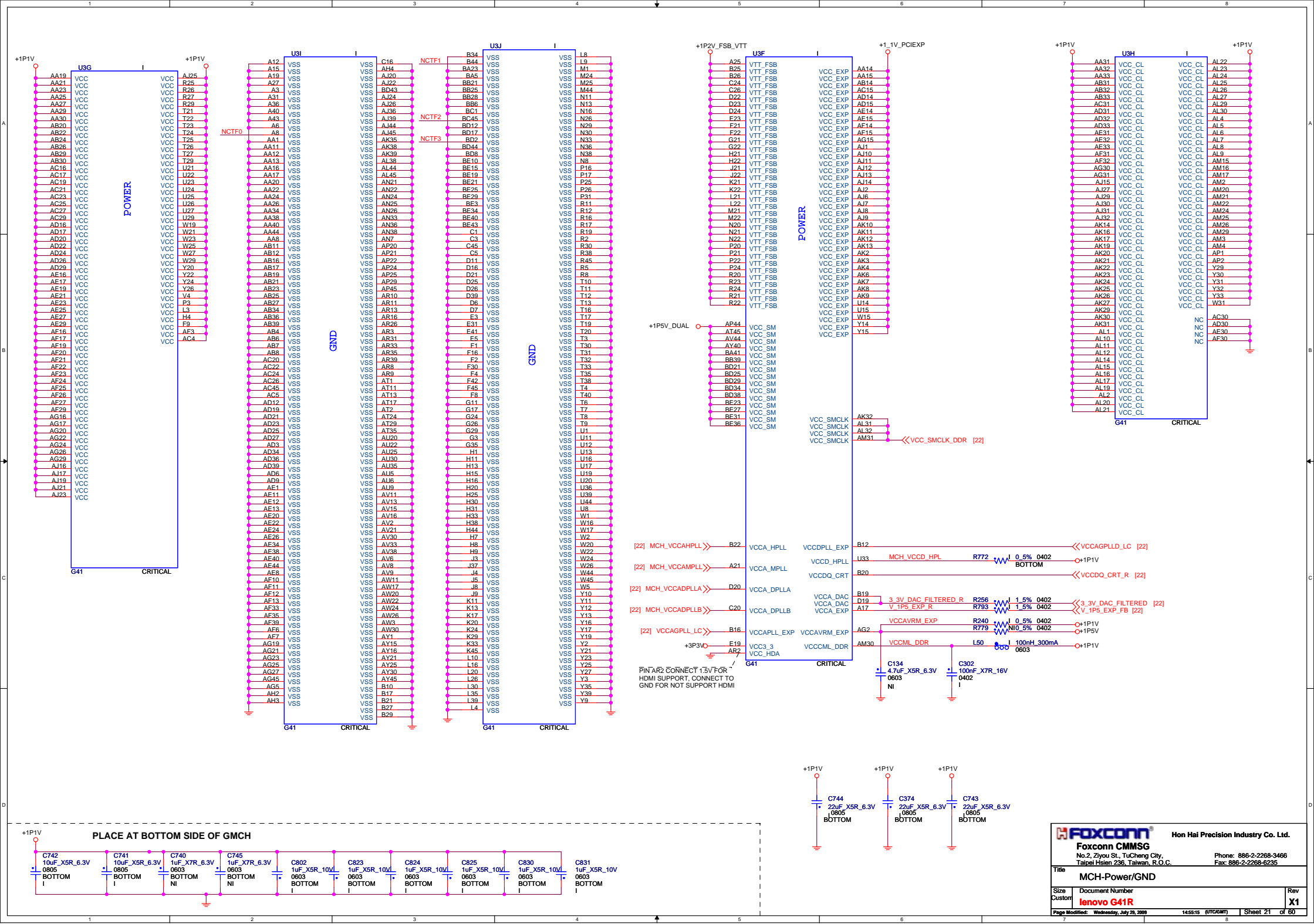
	H	L	DESCRIPTION
EXP_SLR	NORM ●	REVERSE	PCIe LANE NORMAL
EXP_EN_R	ENABLE ●	DISABLE	TLS CONFIDENTIALITY
MCH_SM	ENABLE ●	DISABLE	CONCURRENT PCIe PORT (ENABLE SDVO AND PCIe)



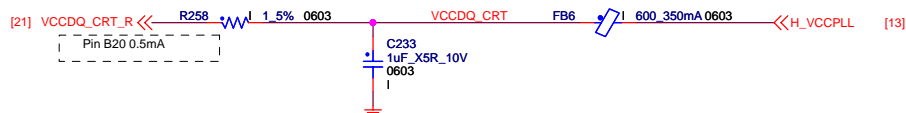
Integrated TPM Straps (DG_V1.3 : Figure12-10)

	Low	High	Float
ENABLE	ITPM_EN(GMCH.L17)	TPM_PP(ICH.C12) SPI_MOSI(ICH.C26)	
DISENABLE	TPM_PP(ICH.C12)		ITPM_EN(GMCH.L17) SPI_MOSI(ICH.C26)

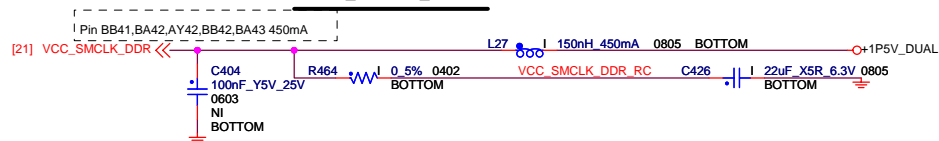




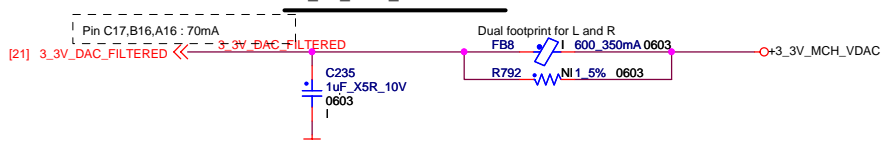
VCCD_CRT



VCC_SMCLK_DDR



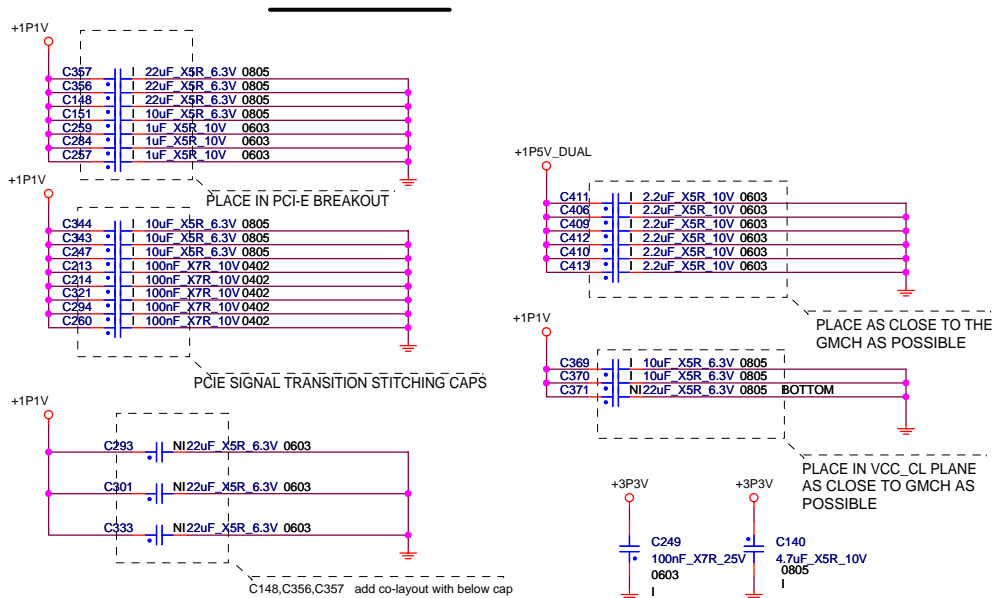
3_3V_DAC_FILTERED



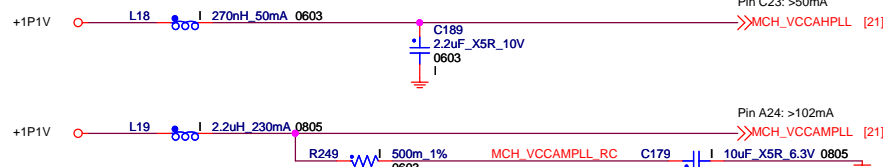
V_1P5_EXP_FB_FILTERED



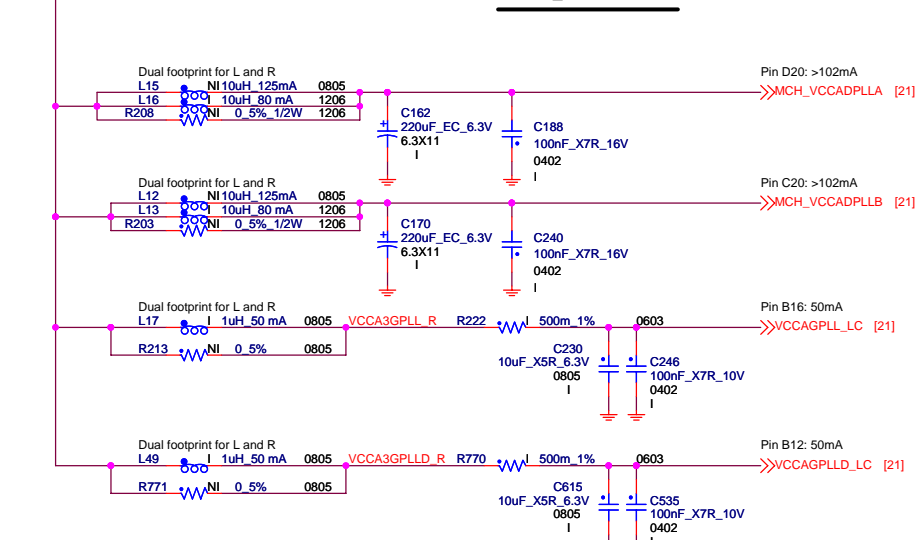
DECOUPLING CAP



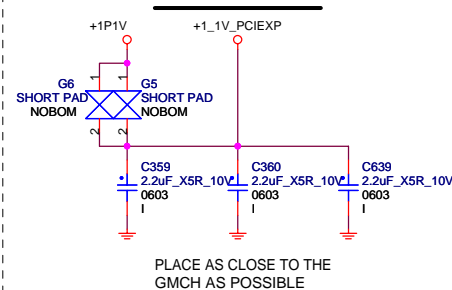
MCH_VCCAPLL



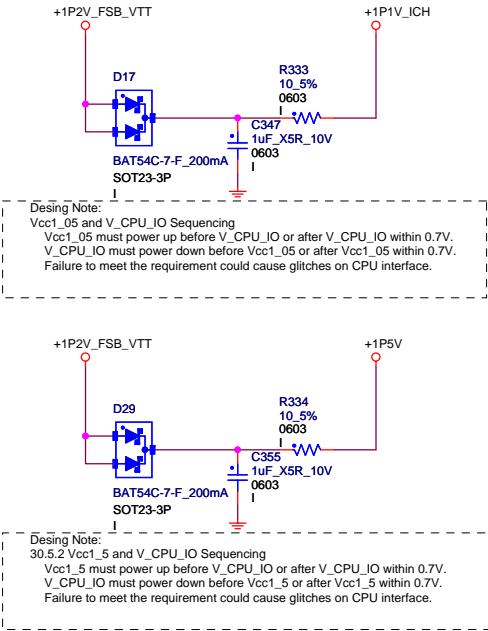
MCH_VCCADPLL



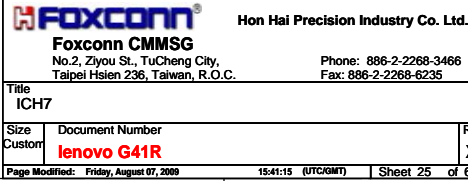
+1P1V_PCIEXP

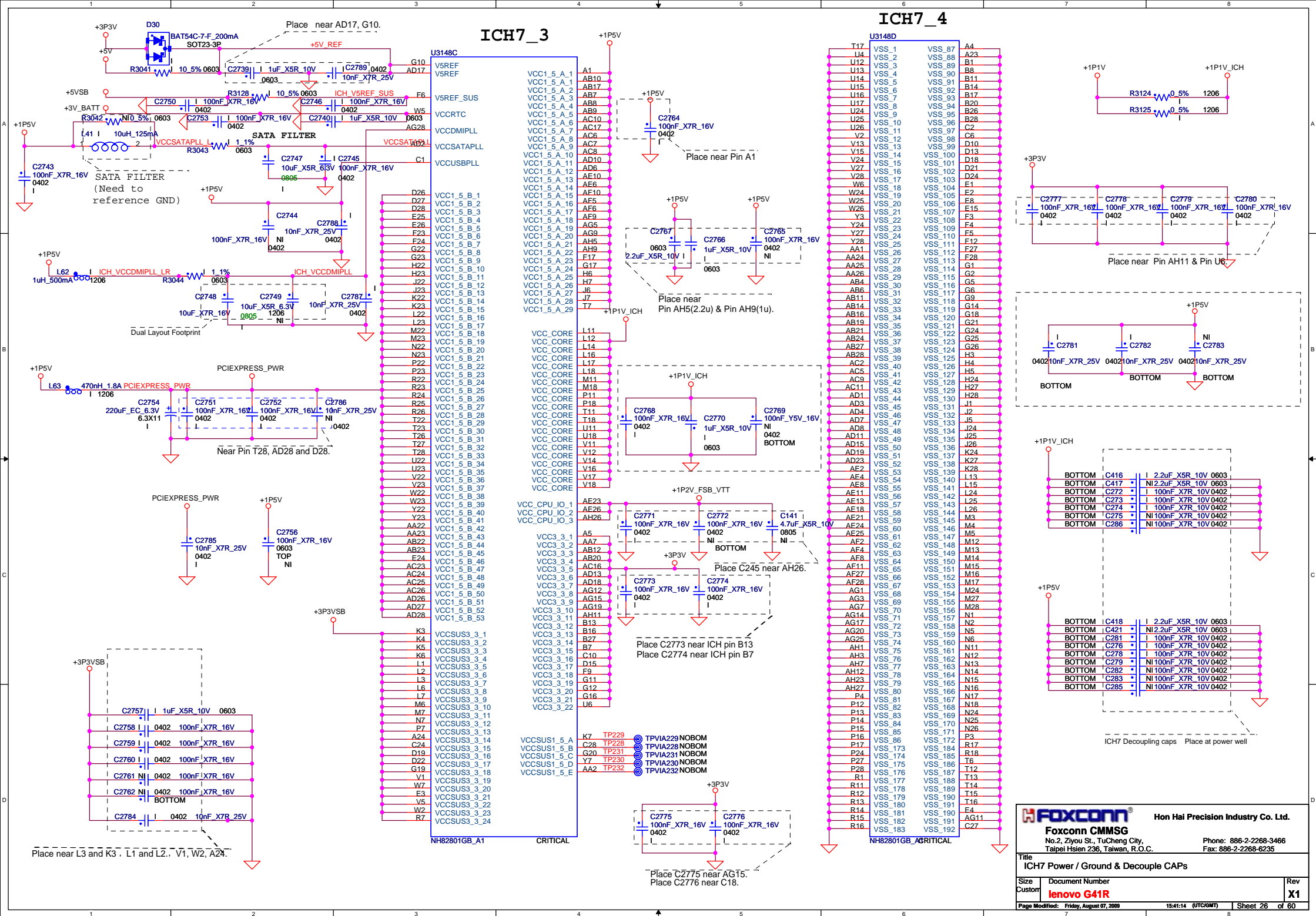


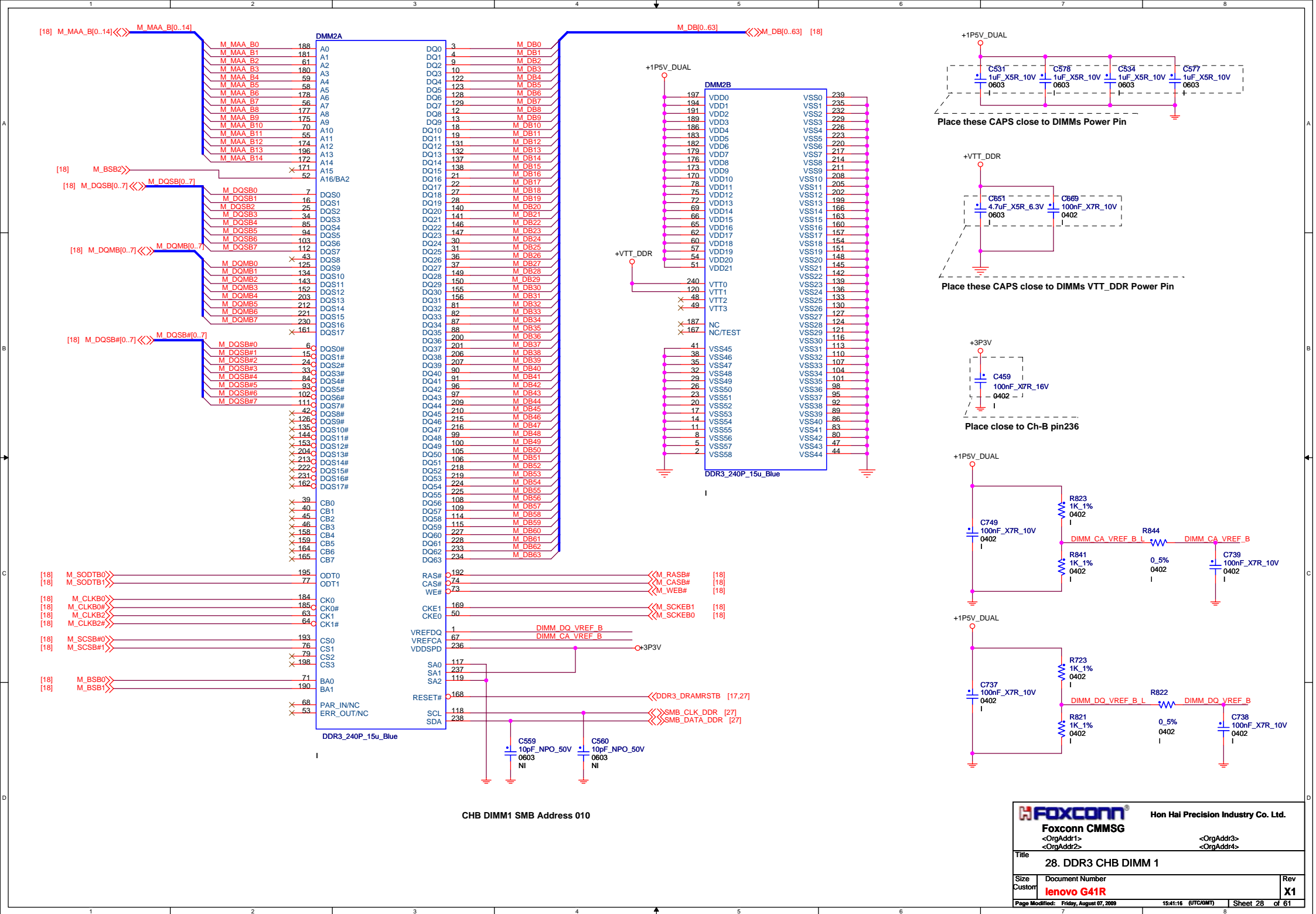
Option For Power Sequence



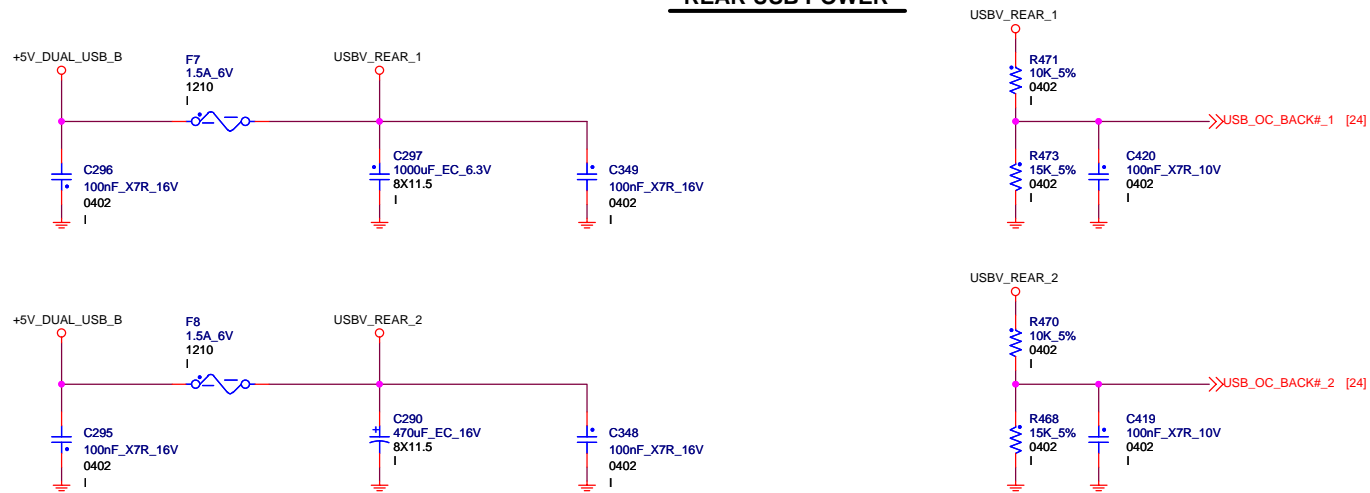
U3148B



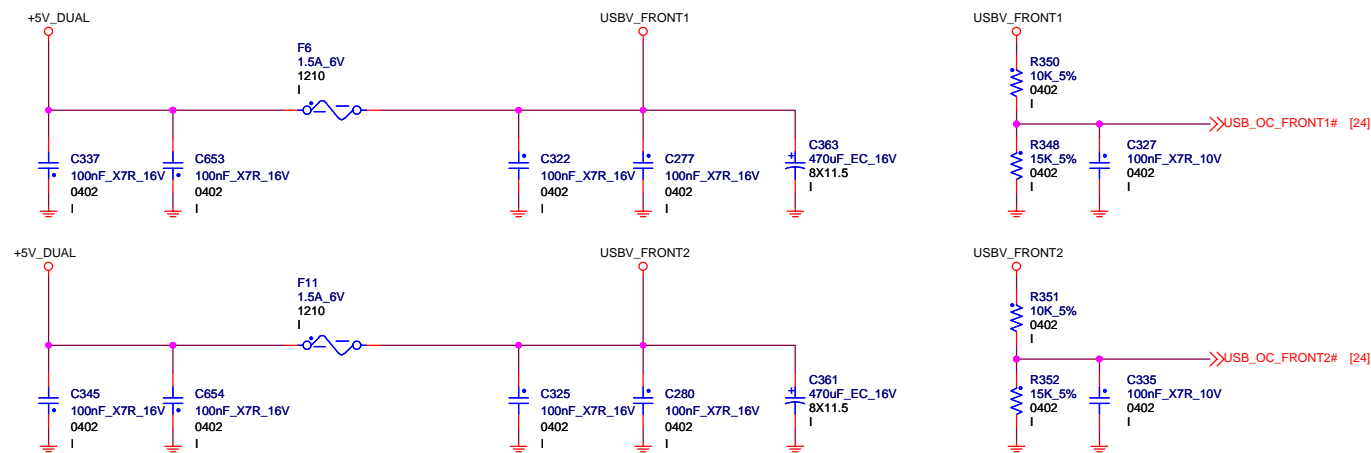


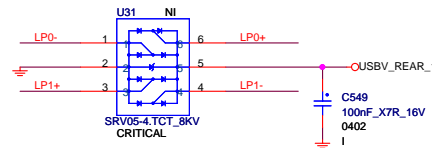
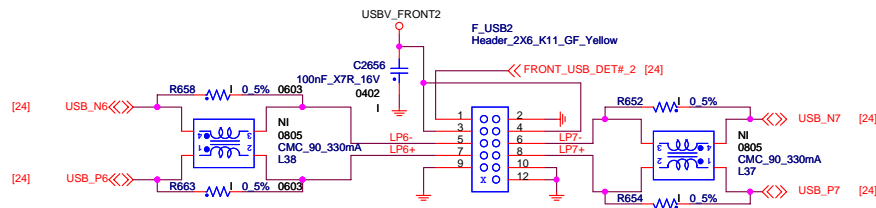
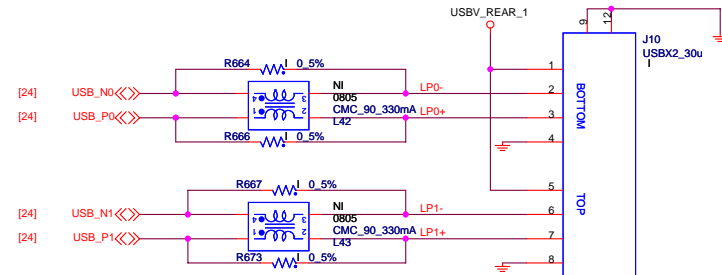
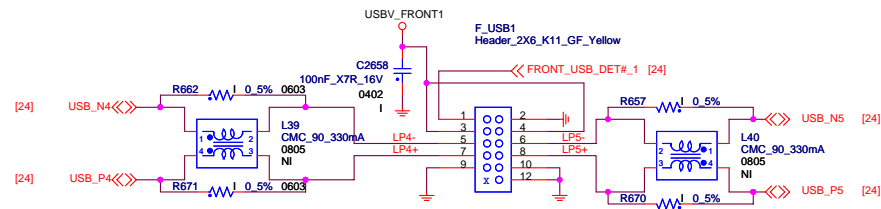


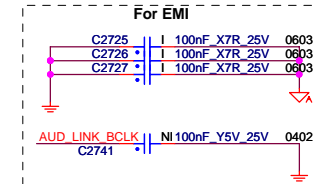
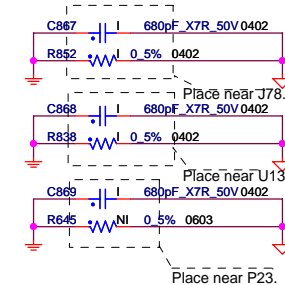
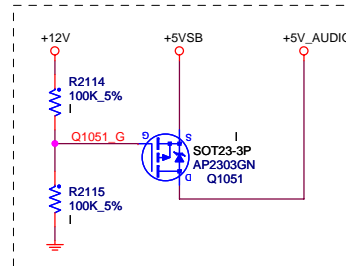
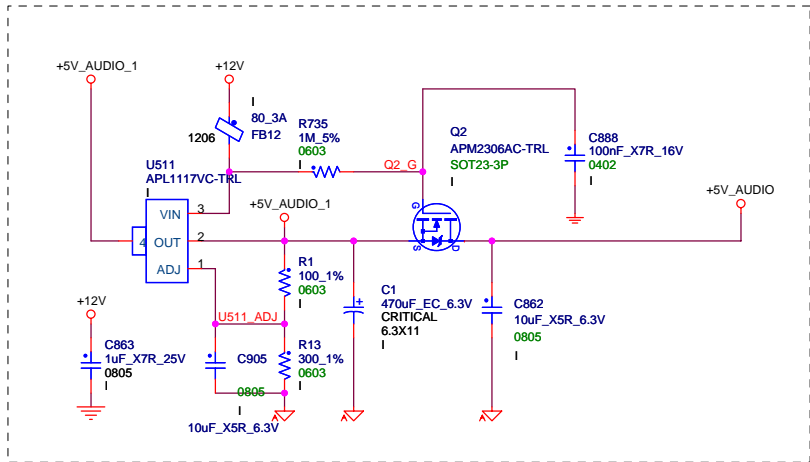
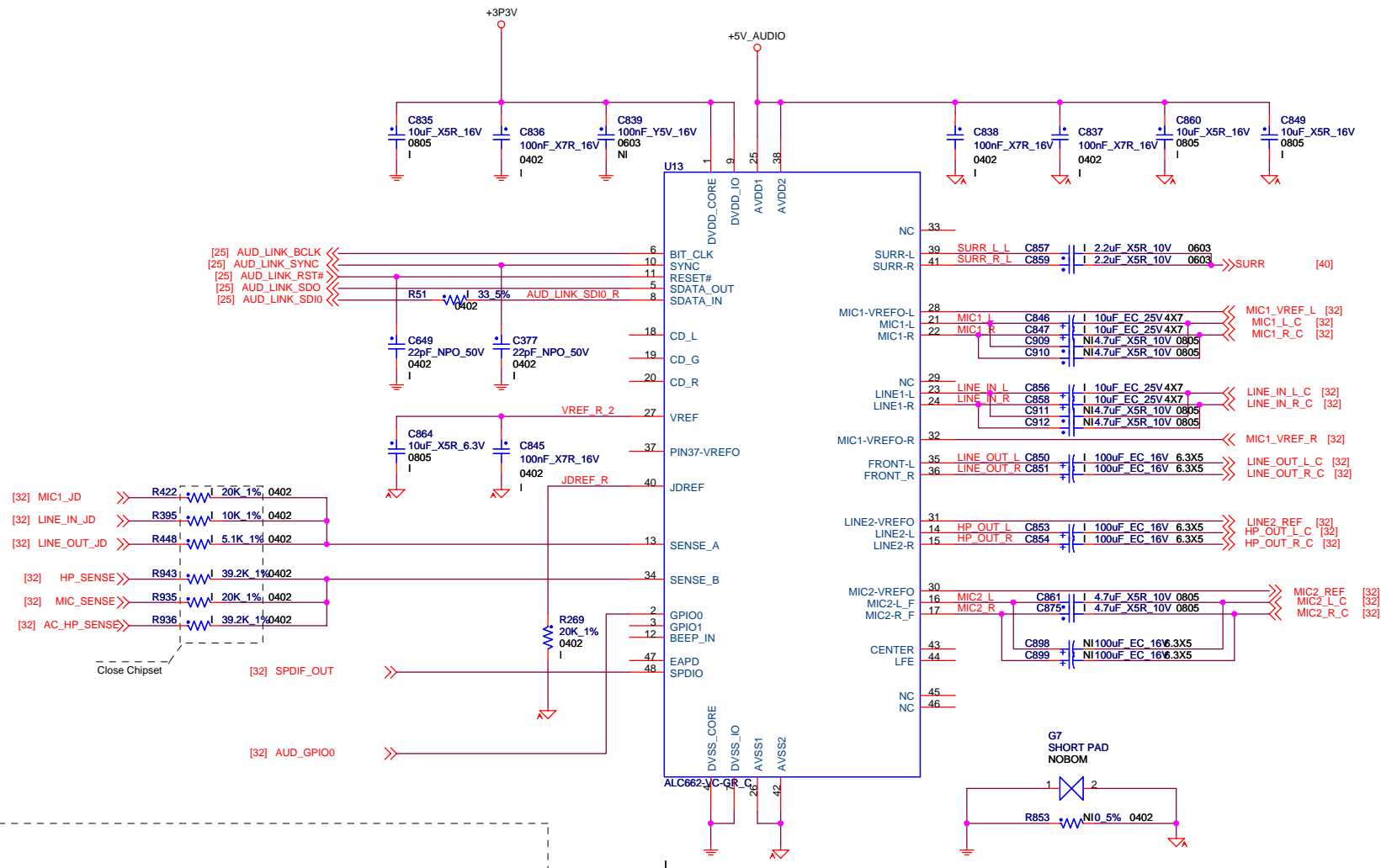
REAR USB POWER

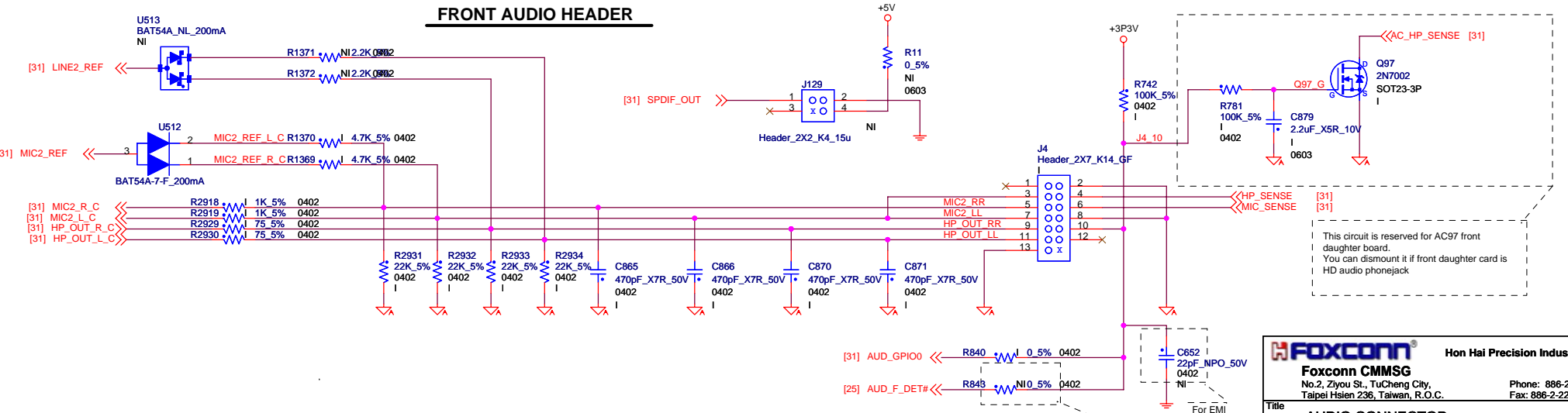
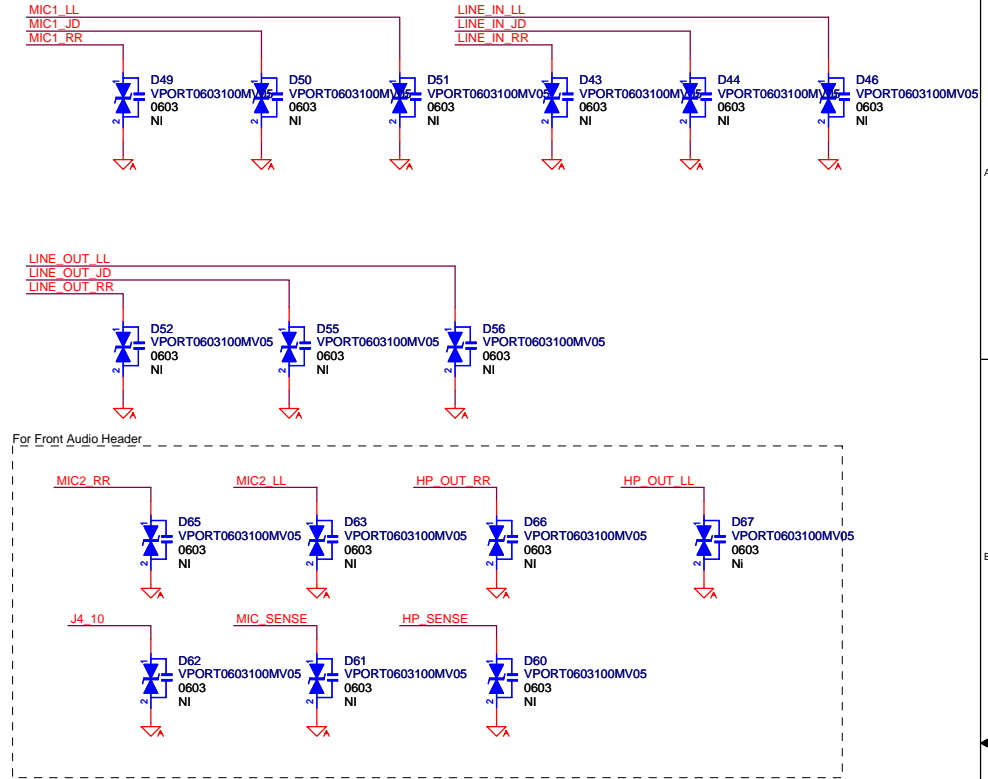
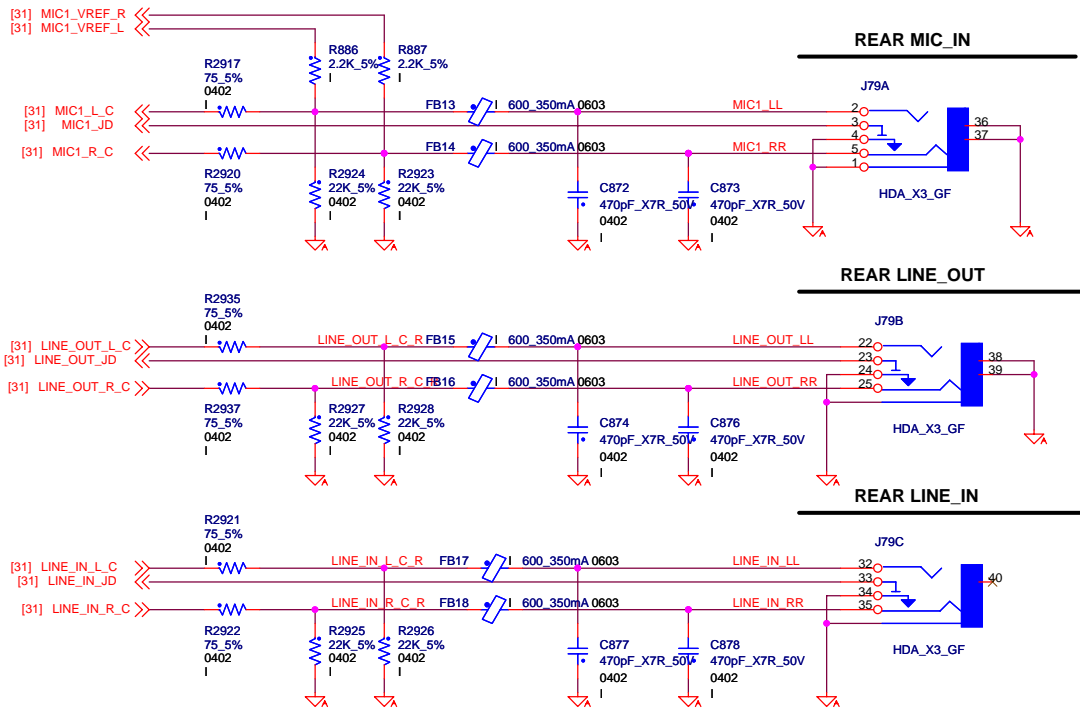


FRONT USB POWER





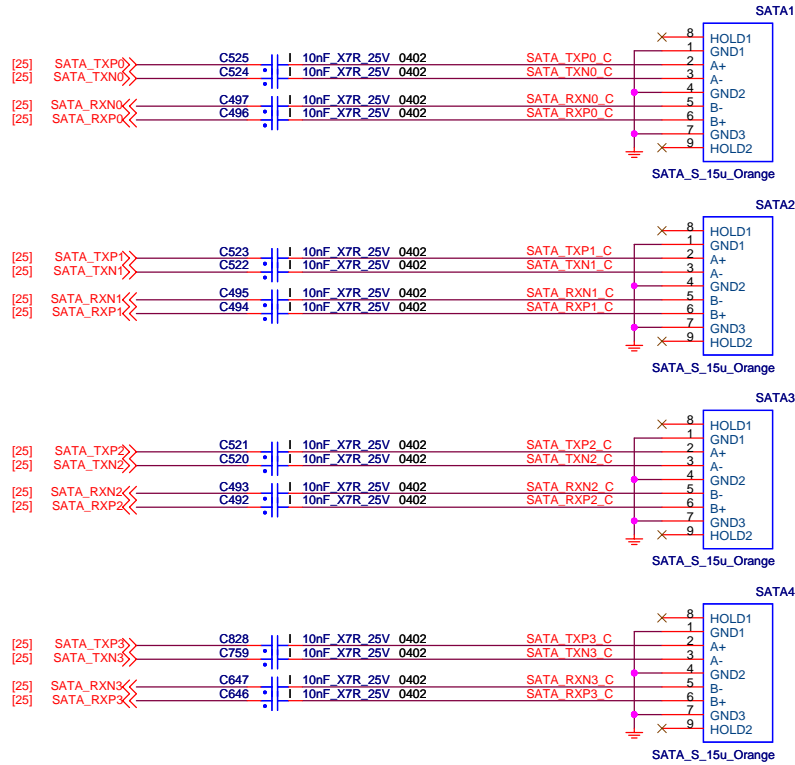




The "AUD_F_DET#" have pull up 8.2K to 3.3V. If enable the function need to remove ICH site pull up resistor.

Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.	
Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
AUDIO CONNECTOR	
Title Size Custon	Document Number lenovo G41R
Page Modified: Friday, August 07, 2009 15:41:15 (UTC+8)	Sheet 32 of 60

SATA



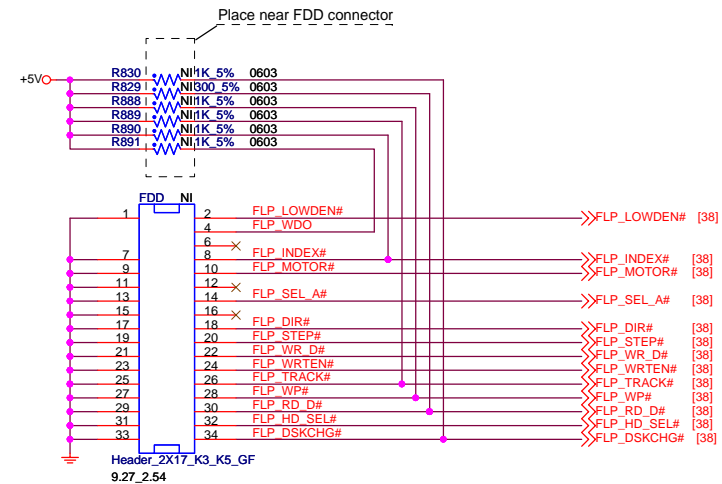
The Primary Hard drive will run off of SATA

SERIAL ATA CAD NOTES:

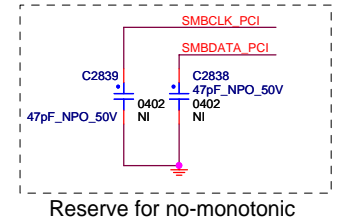
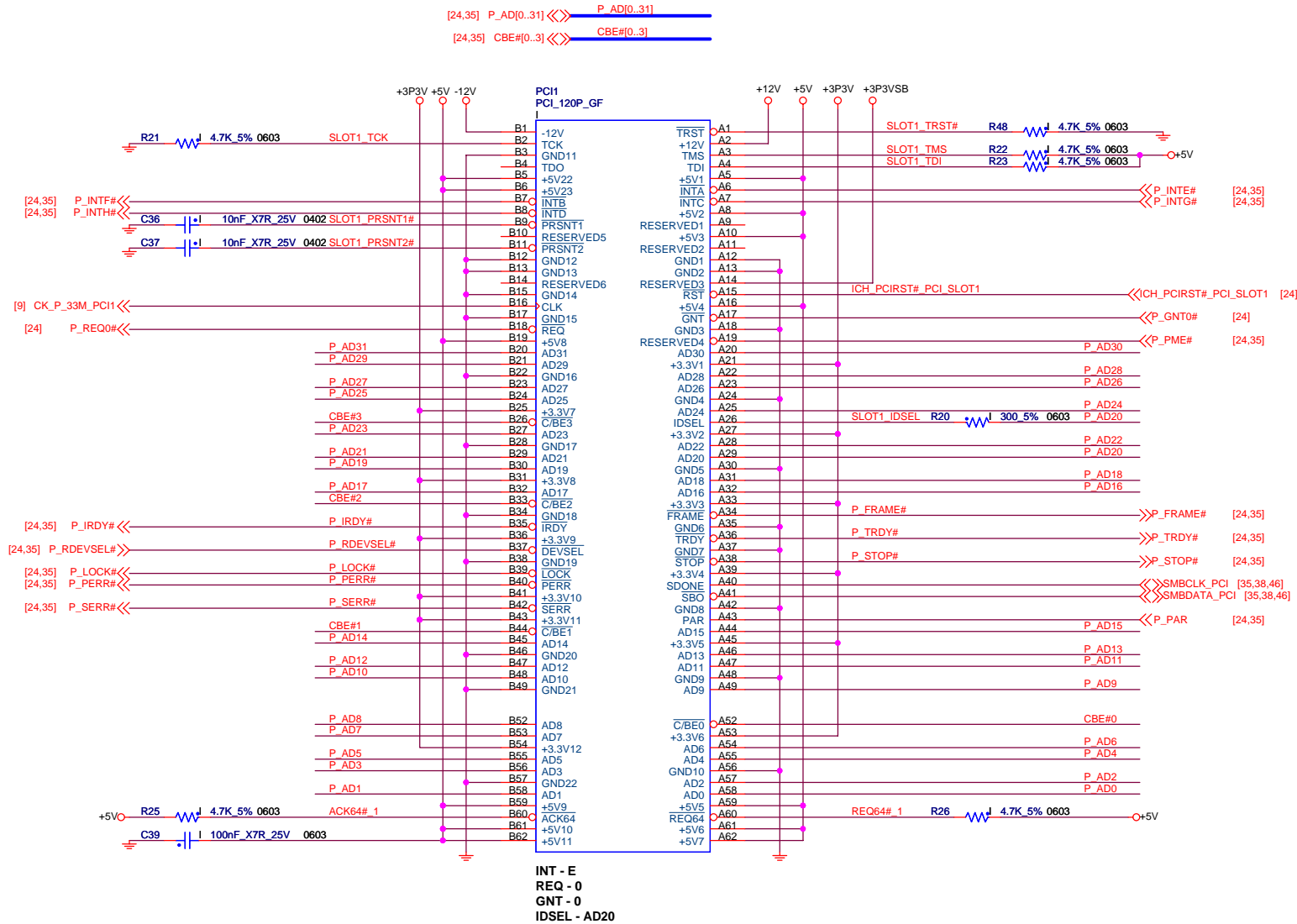
- Serial ATA signals must be referenced to ground
- Minimize layer changes
- Do no route SATA signal under crystals, oscillators, clock synthesizers or magnetic devices.
- SATA spacing is the same as USB 2.0
- Maximum length of SATA is 3.8" with length mismatched to 20 mils within pair.

FDD

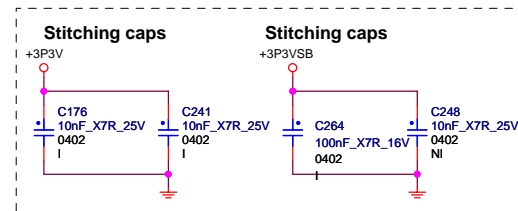
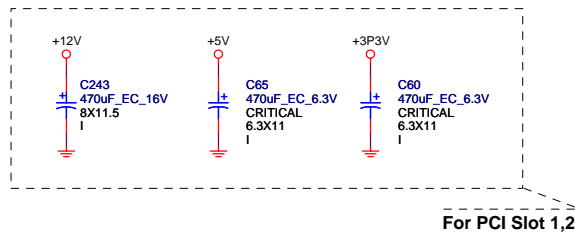
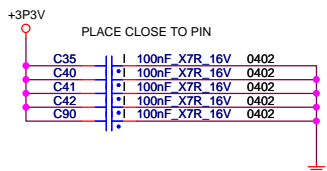
Board only supports one floppy drive.
Must be a twisted floppy cable.



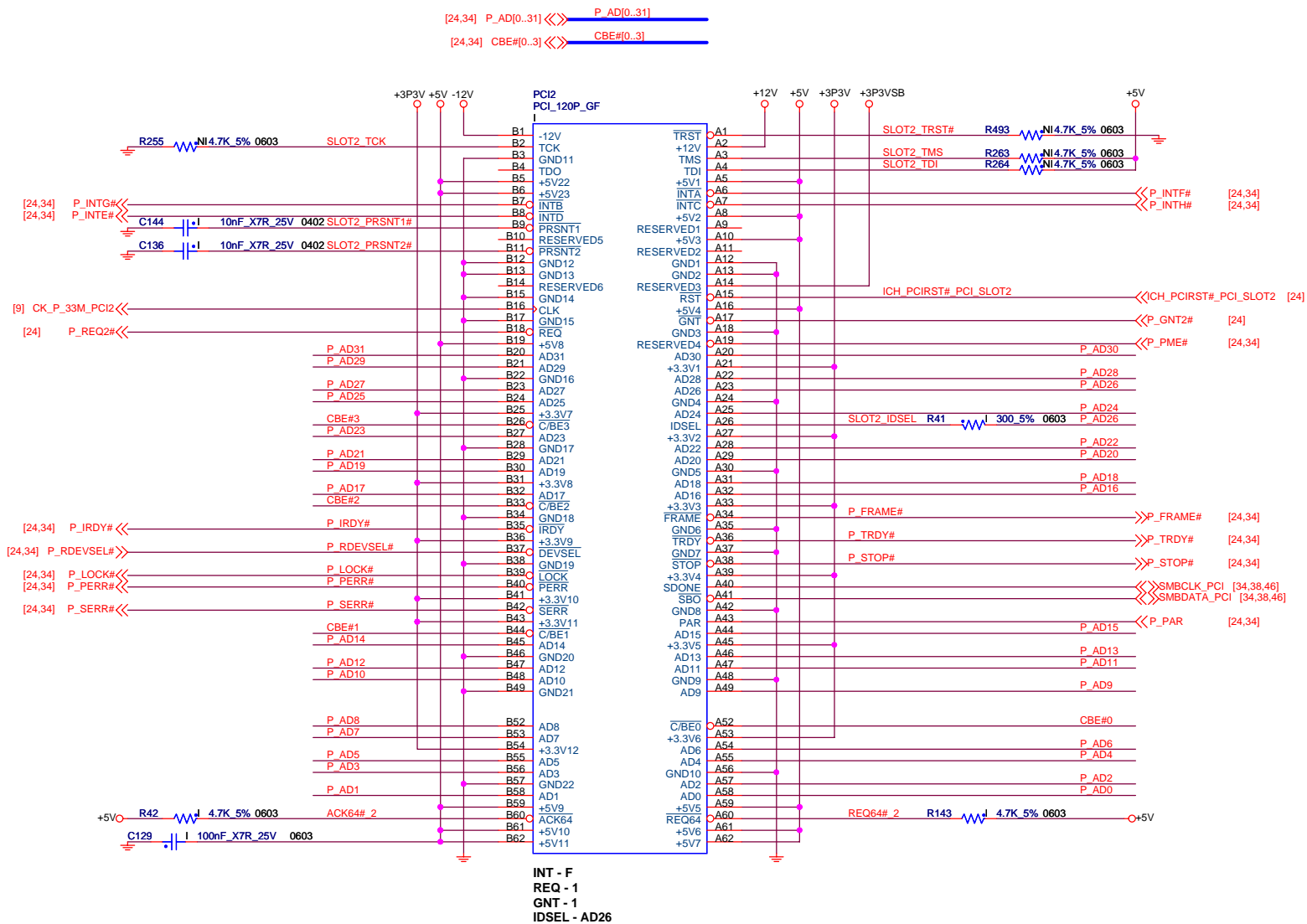
PCI SLOT 1



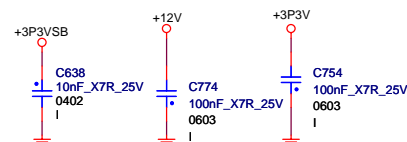
Reserve for no-monotonic



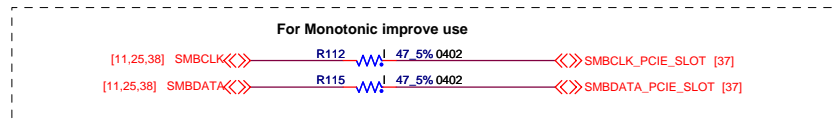
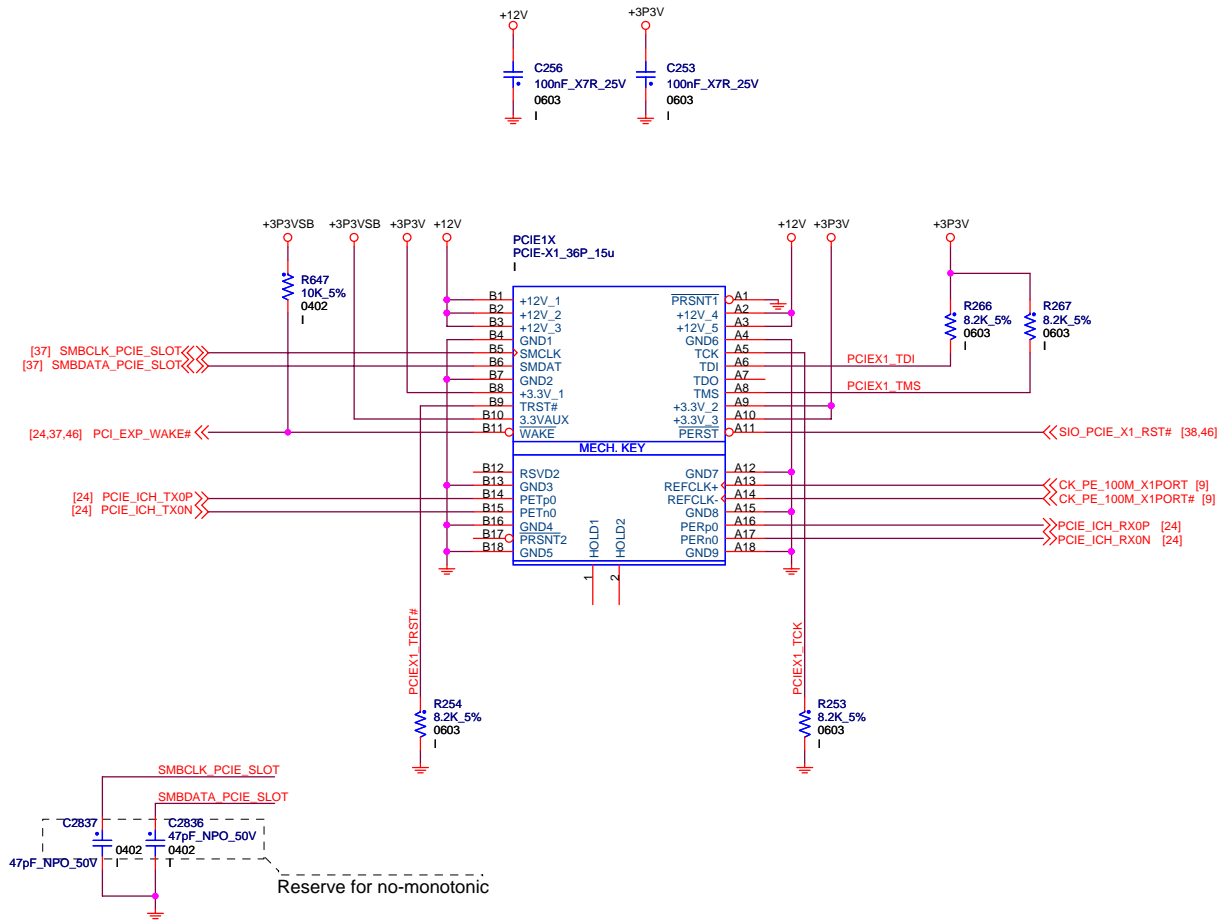
PCI 2 SLOT



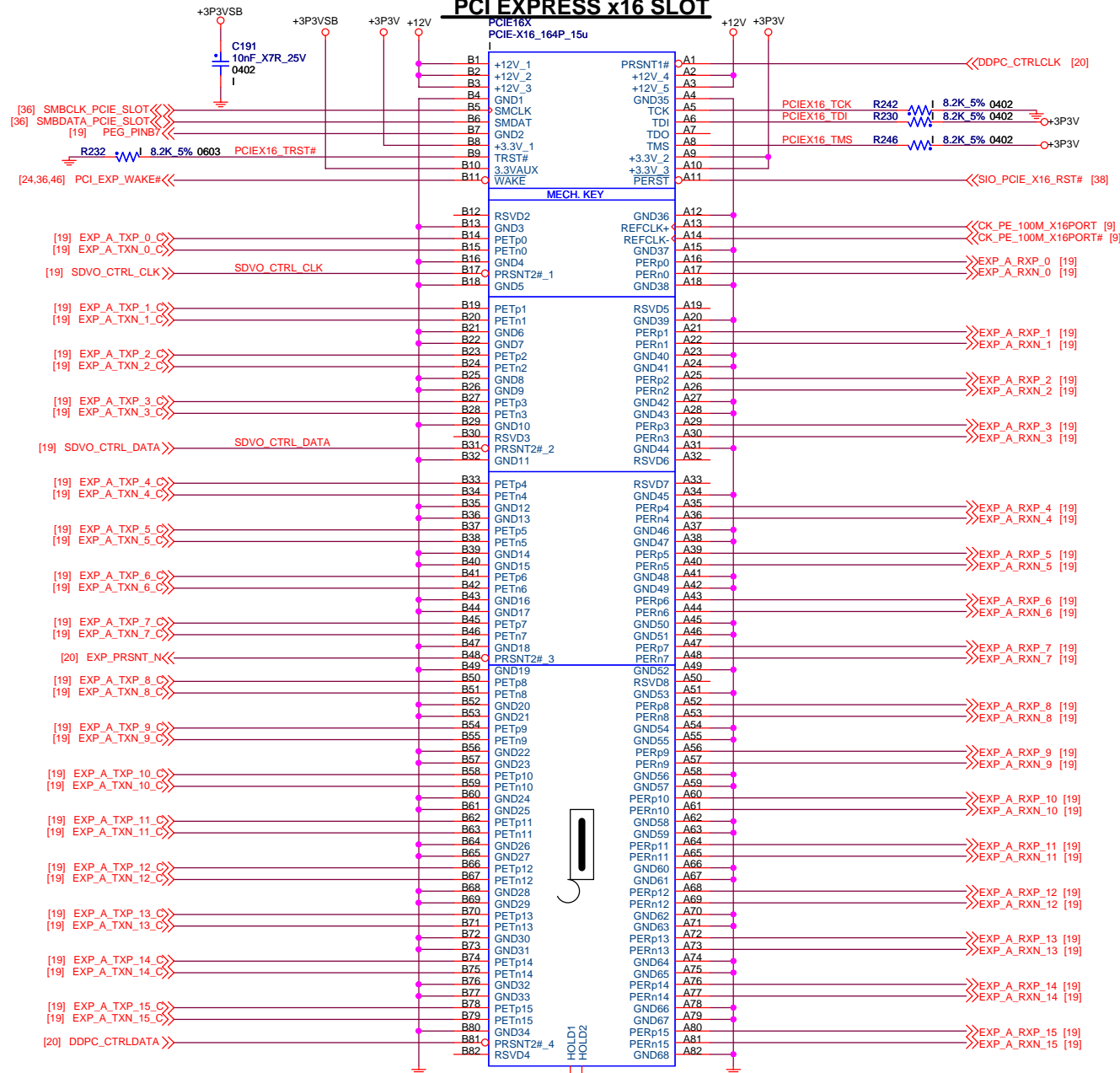
INT - F
REQ - 1
GNT - 1
IDSEL - AD26



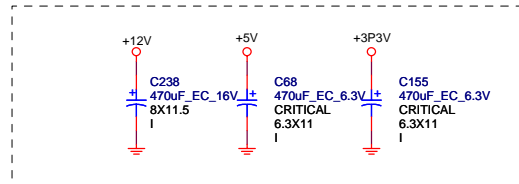
PCI EXPRESS X1 SLOT



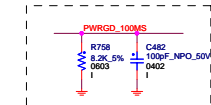
PCI EXPRESS x16 SLOT



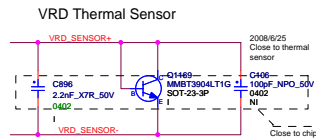
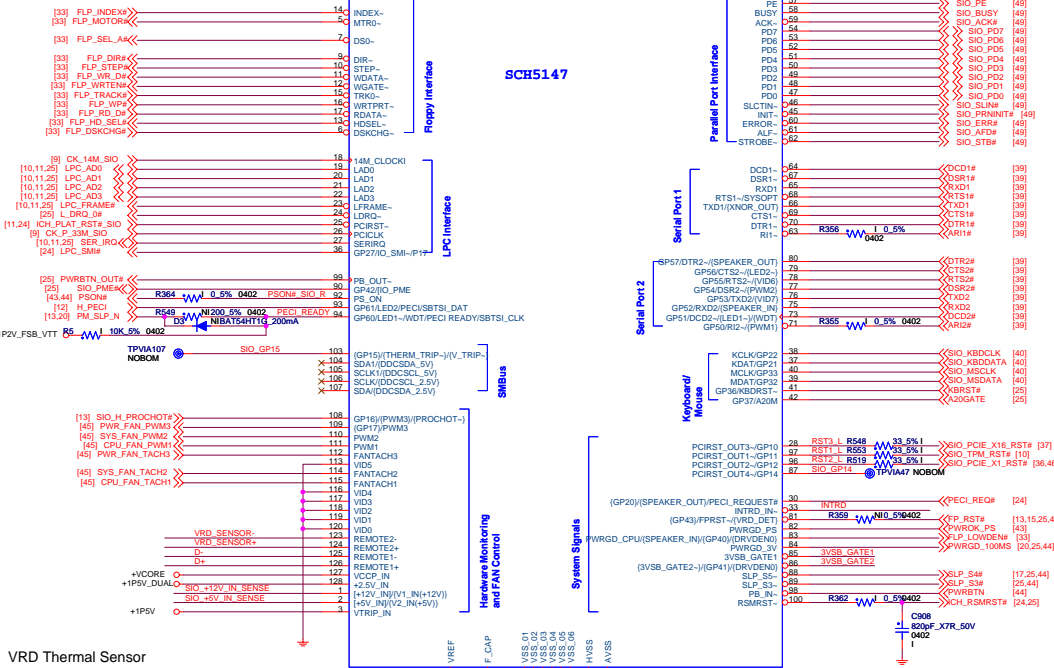
For PCIE x1 and x16 SLOT



Check VBAT Pin define

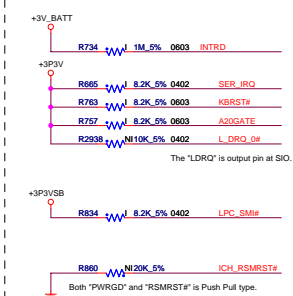
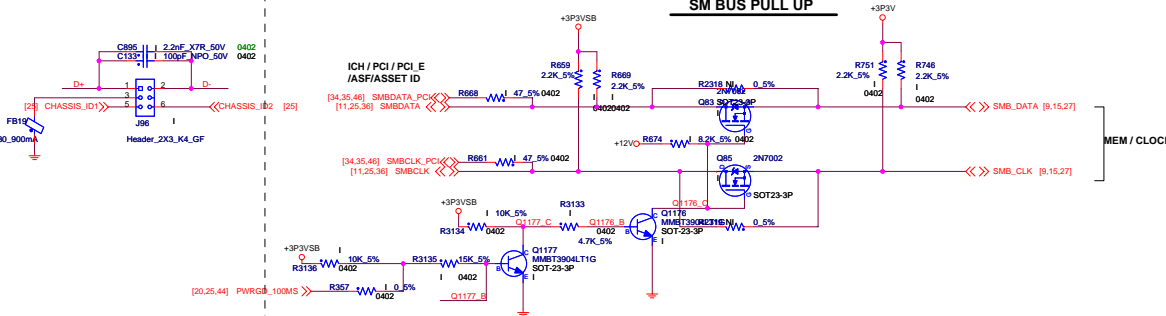


For Gilch free.

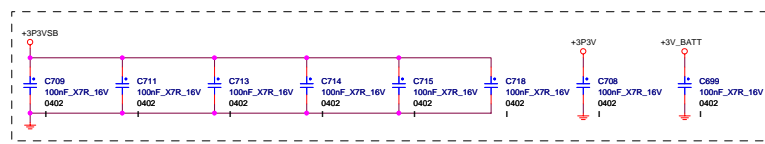
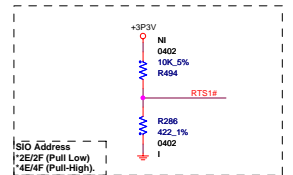
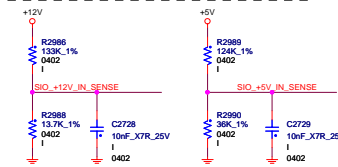


Thermal Header

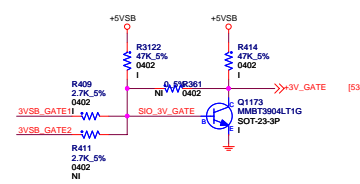
Close to chipset end

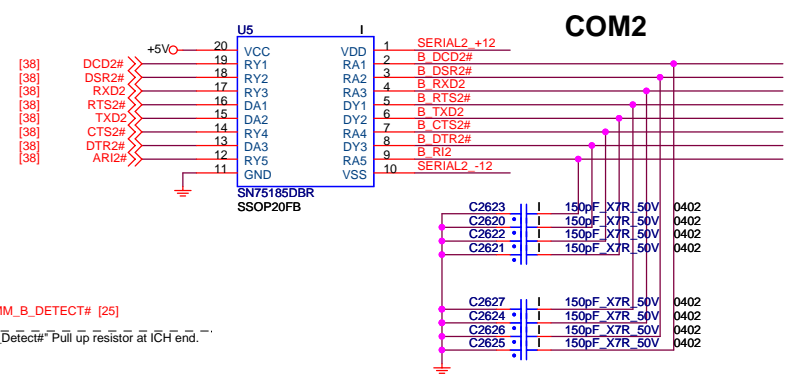
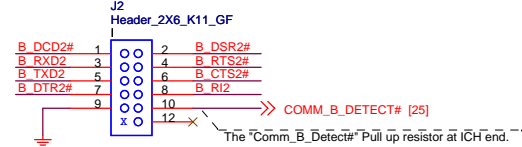
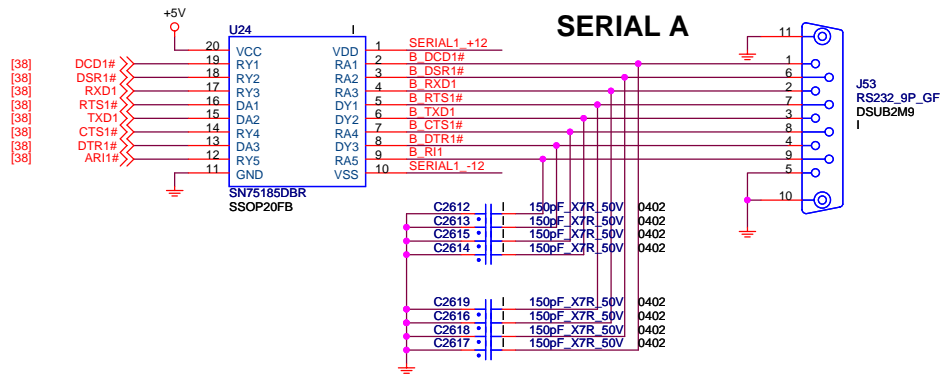


The "LDRQ" is output pin at SIO.

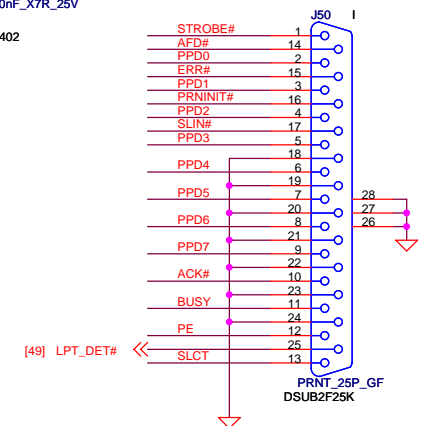
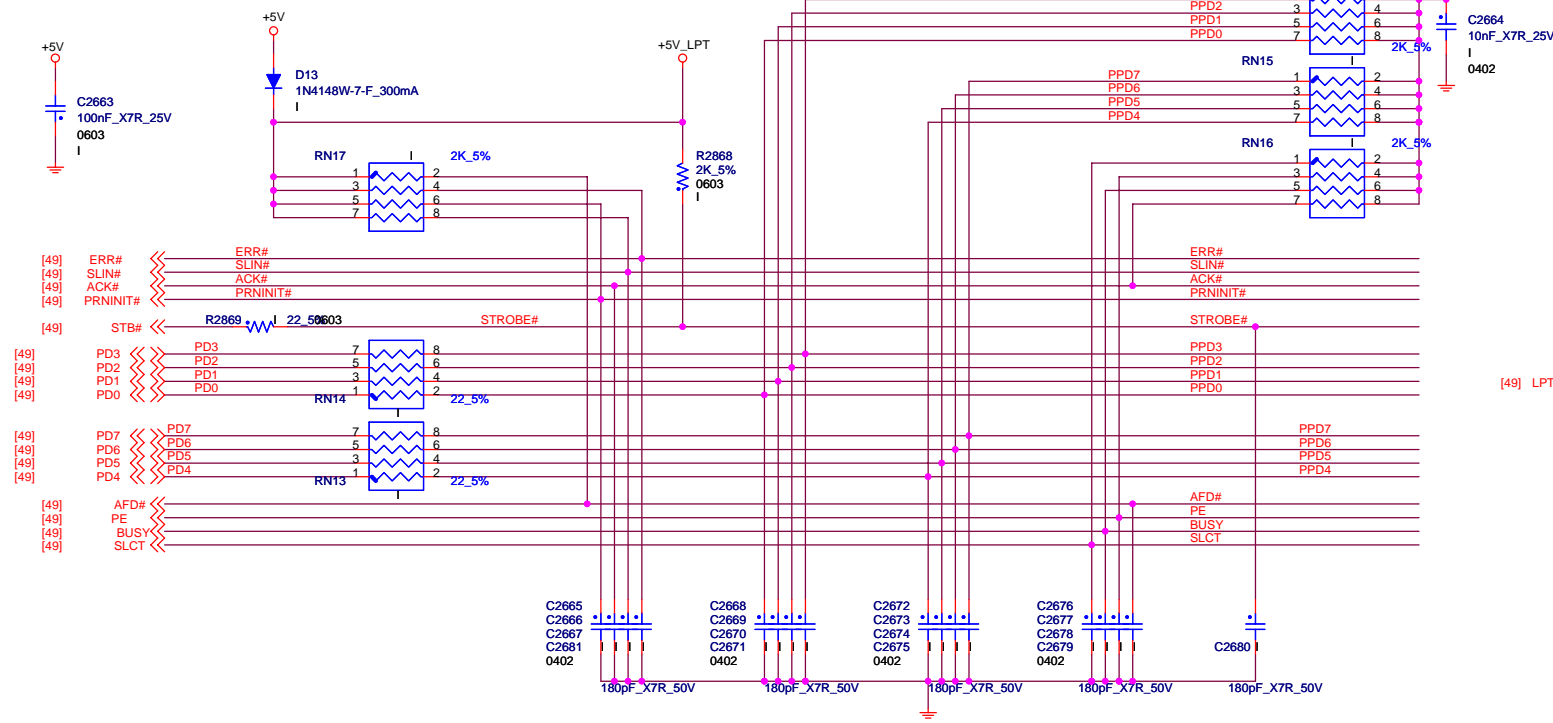
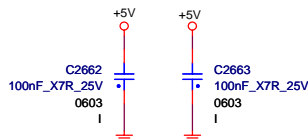
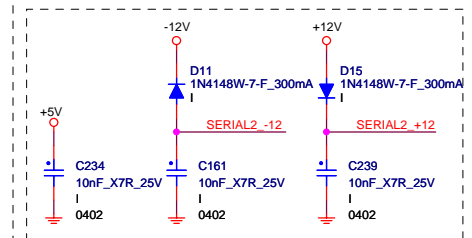
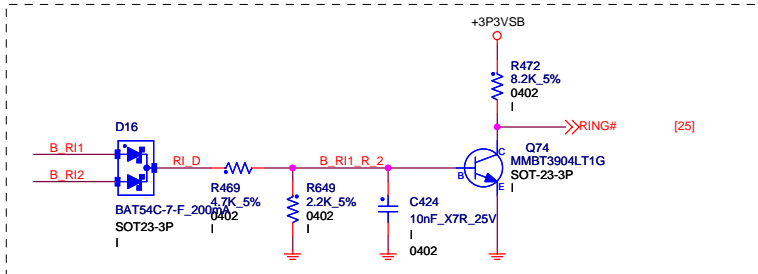
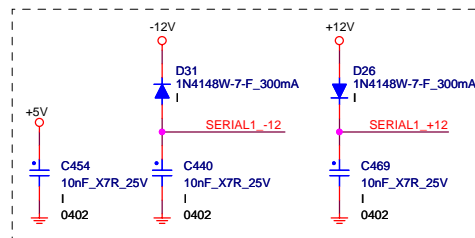


ACPI Control Option

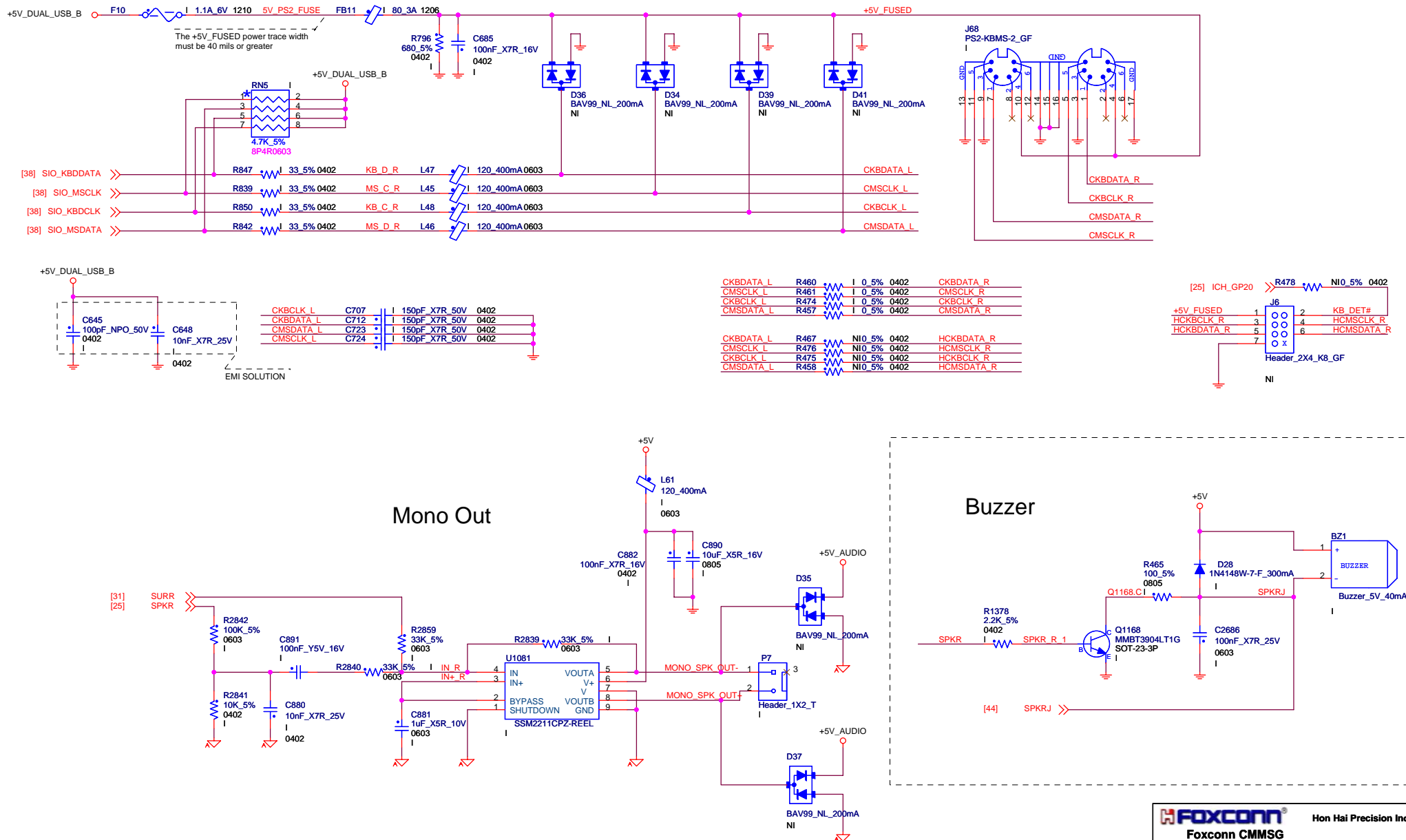


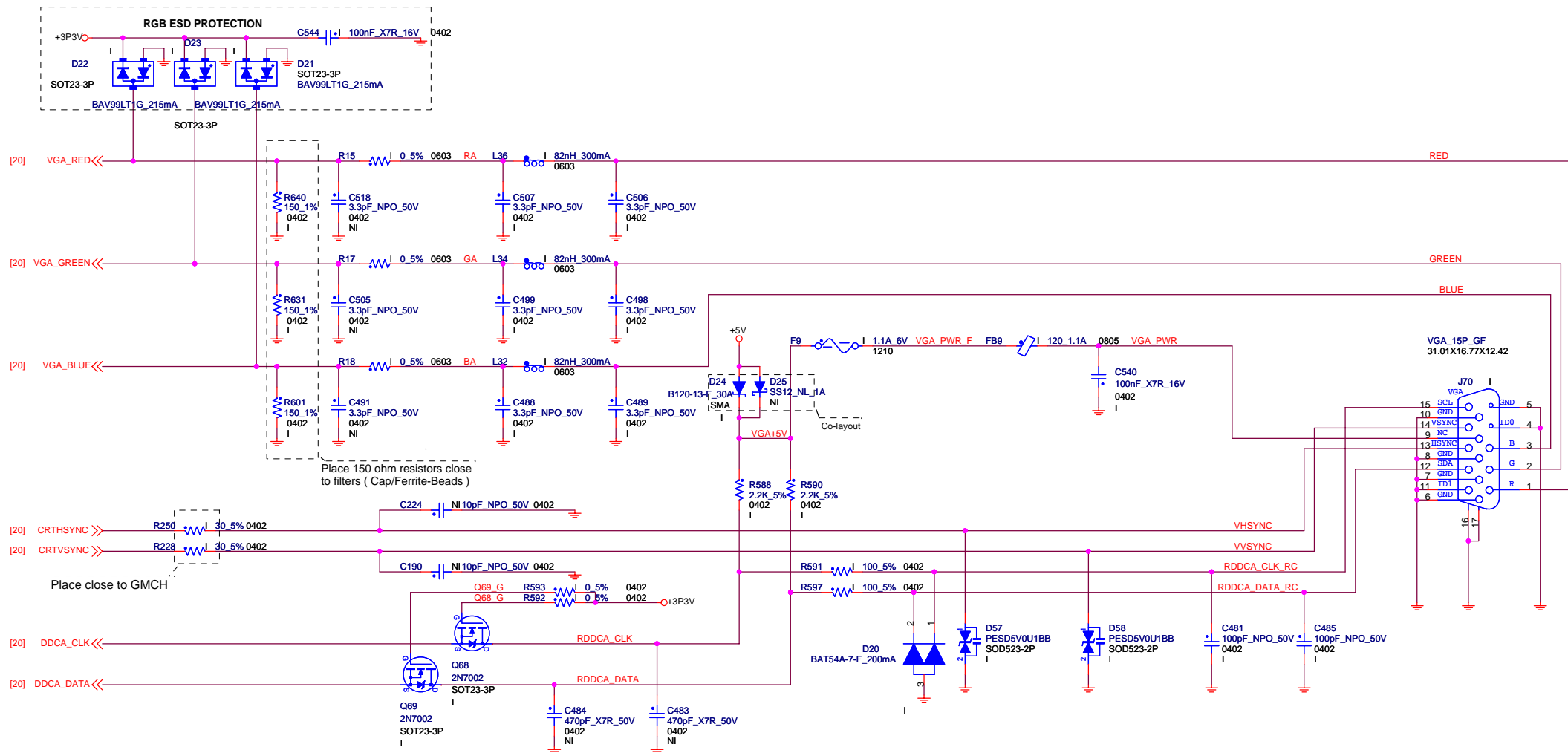


Place caps close to U22

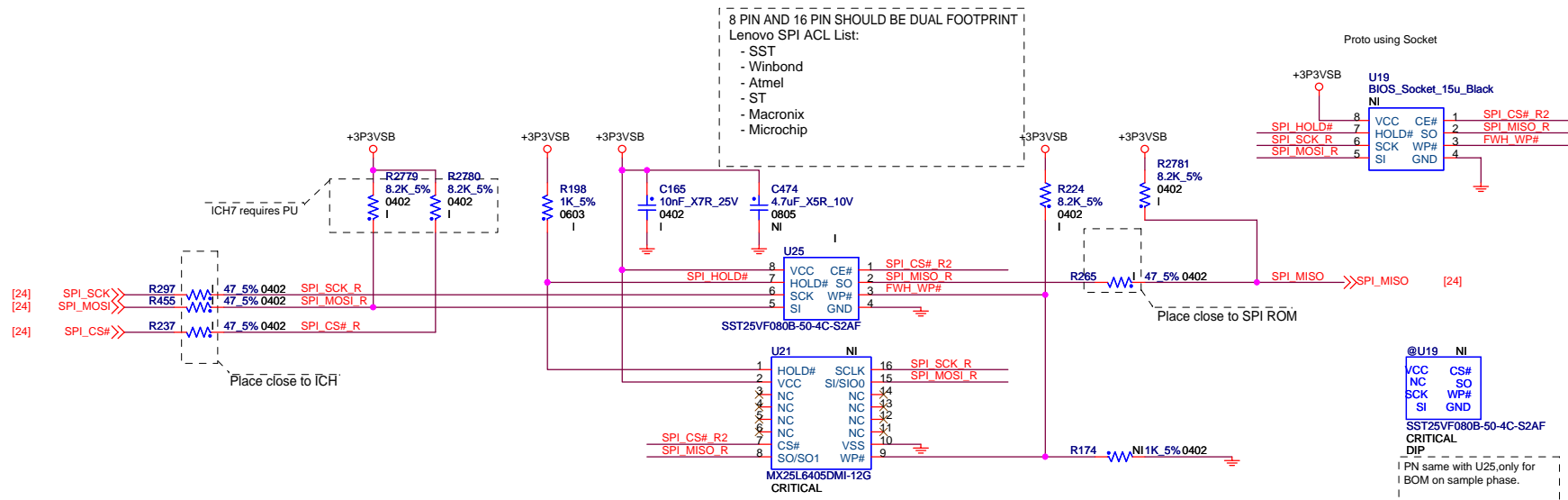


KEYBOARD / MOUSE

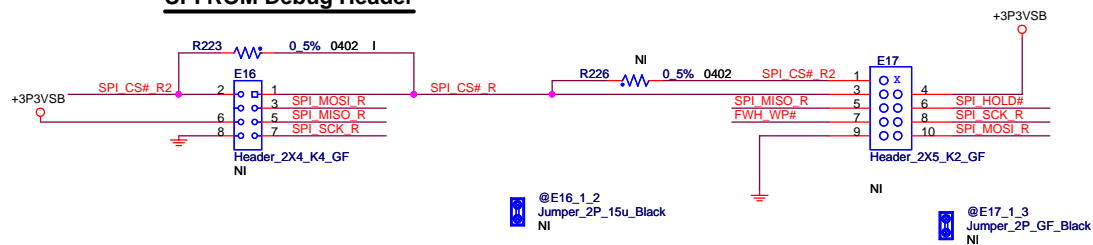




SPI ROM

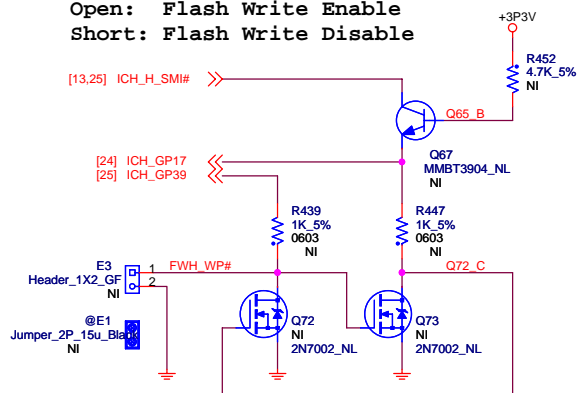


SPI ROM Debug Header

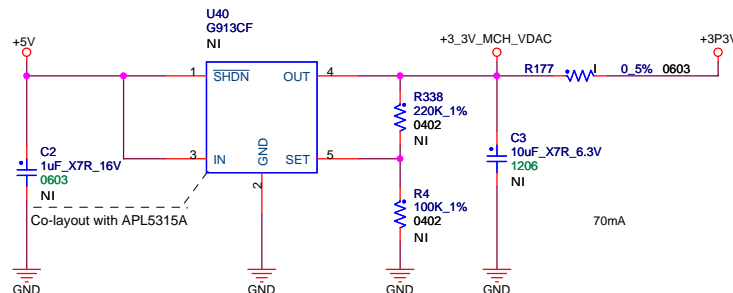


BIOS WRITE PROTECT

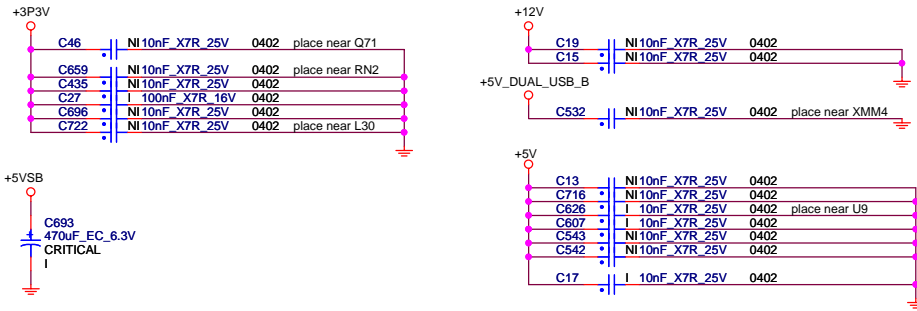
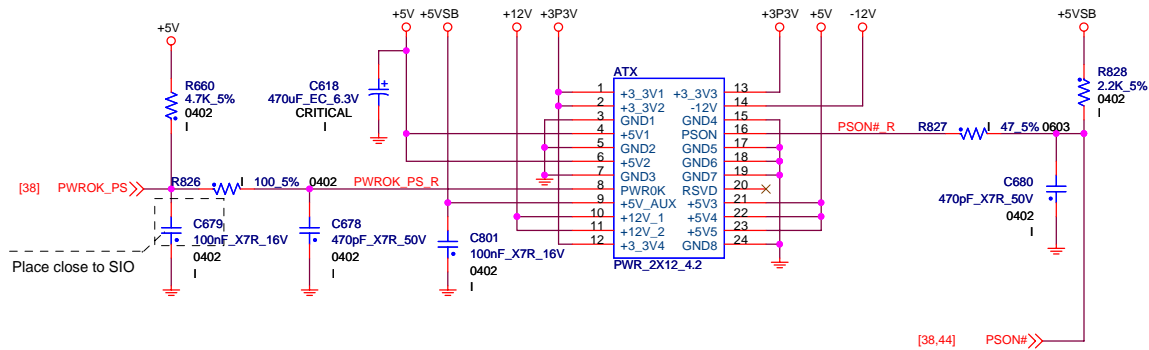
Open: Flash Write Enable
Short: Flash Write Disable



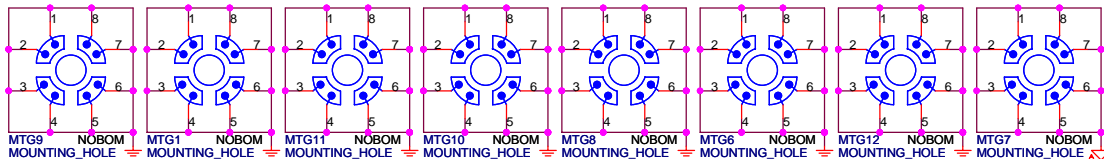
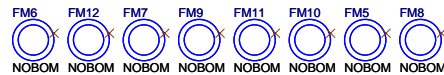
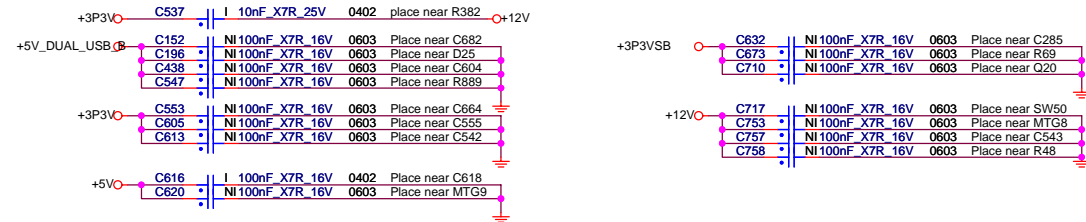
$$V_{out} = 0.8 \times (1 + 220/100) = 3.36$$



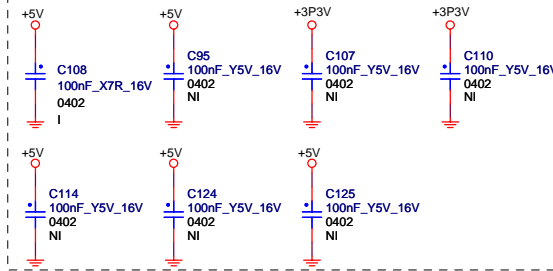
Power Input Connector



EMI Cap

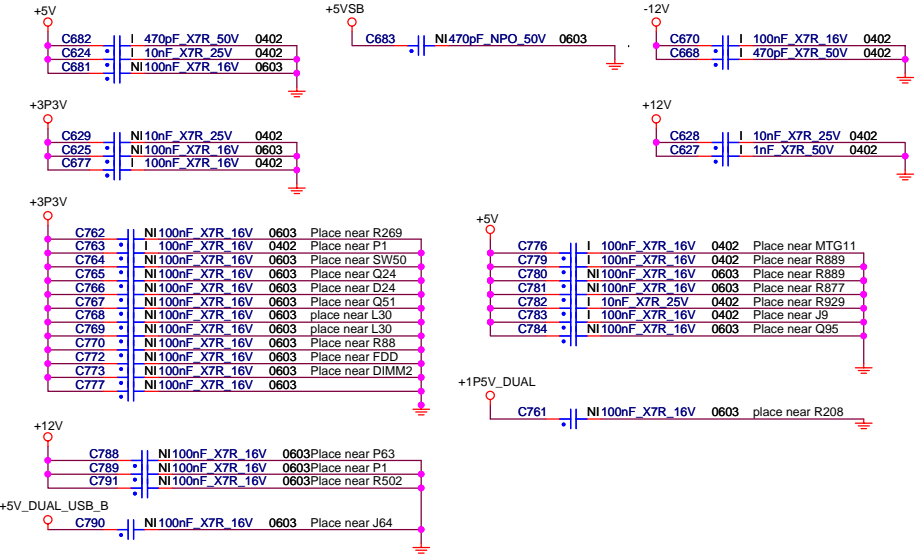


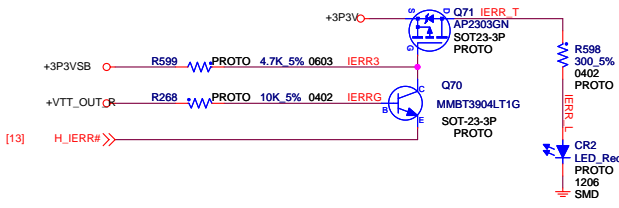
EMI Tony Recommendation 3/7



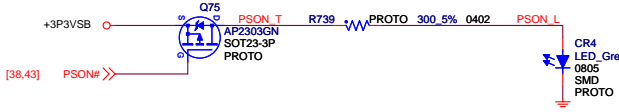
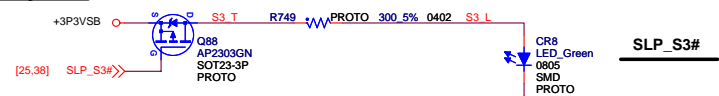
EMI Cap

CAD NOTE:
Place Around the Input Power Connectors

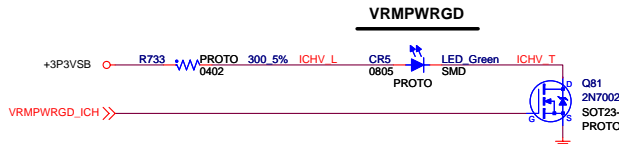
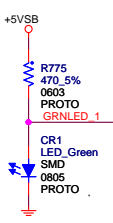




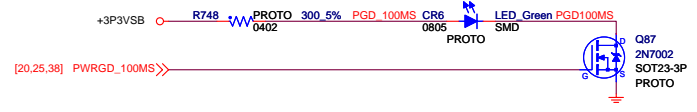
PCA LED For Debug Only



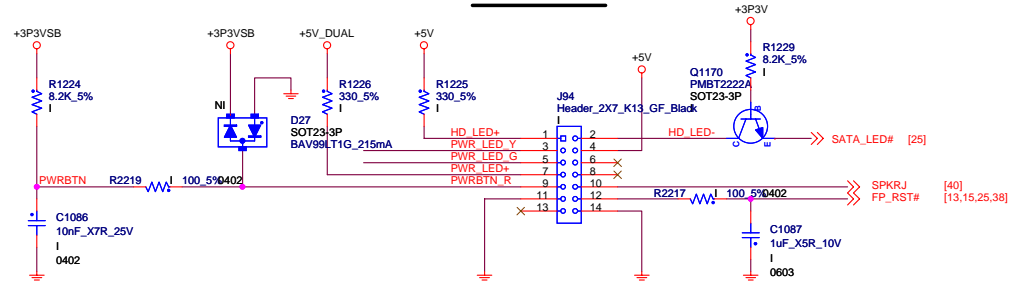
IERR +5V_AUX LED



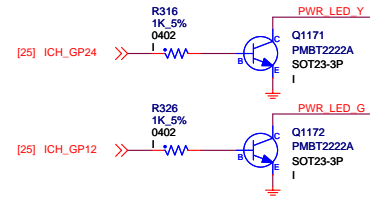
PWRGD_140MS



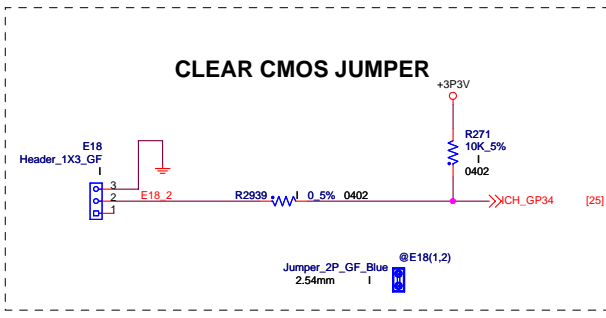
Front Panel



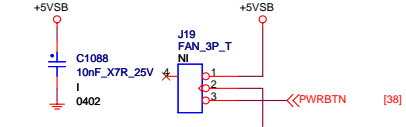
- 3 Pin LED Status**
- S0 (Steady Green)
 - S1 (Green Blinking 1Hz/S)
 - S3 (Steady Yellow)
 - S4/S5 (Off)
- 2 Pin LED Status**
- S0 (Steady Green)
 - S1/S3 (Blinking 1Hz/S)
 - S4/S5 (Off)



CLEAR CMOS JUMPER



FRISW



FOXCONN Hon Hai Precision Industry Co. Ltd.

Foxconn CMMSG
No.2, Ziyou St., TuCheng City,
Taipei Hsien 236, Taiwan, R.O.C.

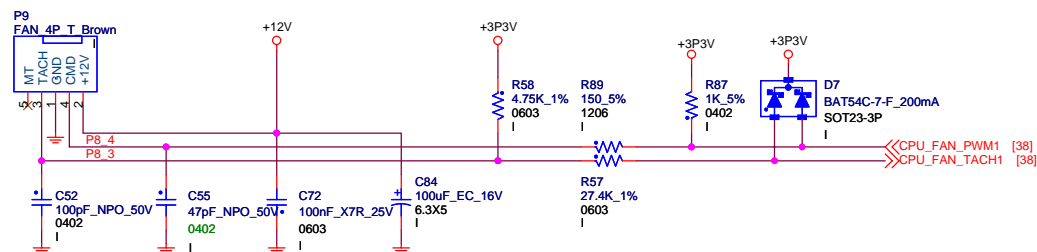
Phone: 886-2-2268-3466
Fax: 886-2-2268-6235

Title: **PCA LED Circuit**

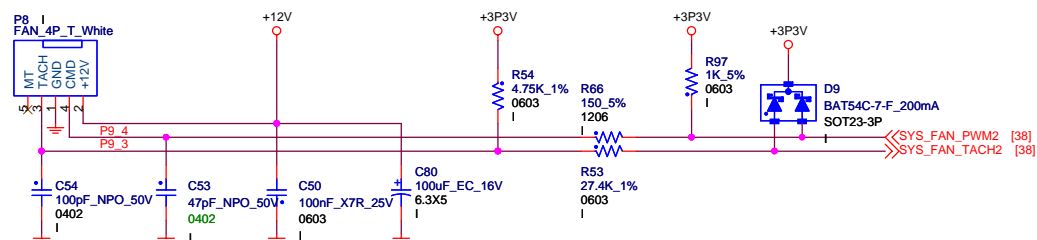
Size	Document Number	Rev
Custom	lenovo G41R	X1

Page Modified: Wednesday, July 25, 2009 15:34:35 (UTC+8) Sheet 44 of 60

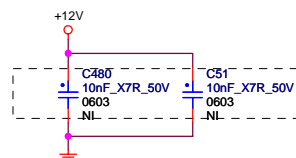
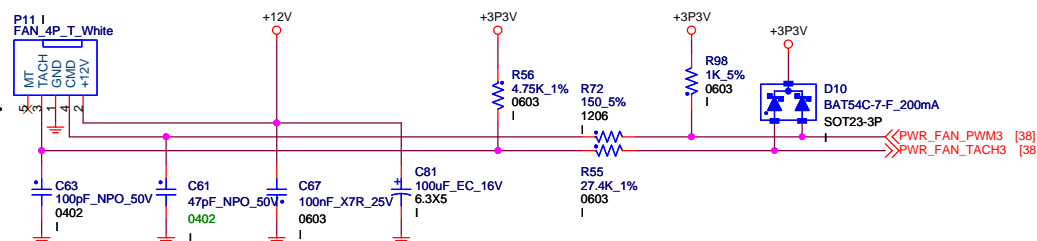
Color: Brown



Color: White

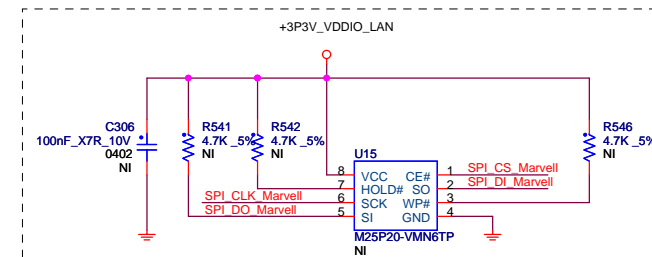
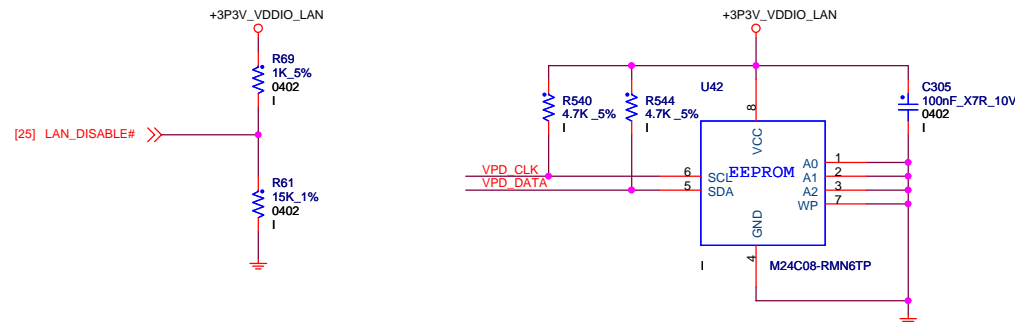
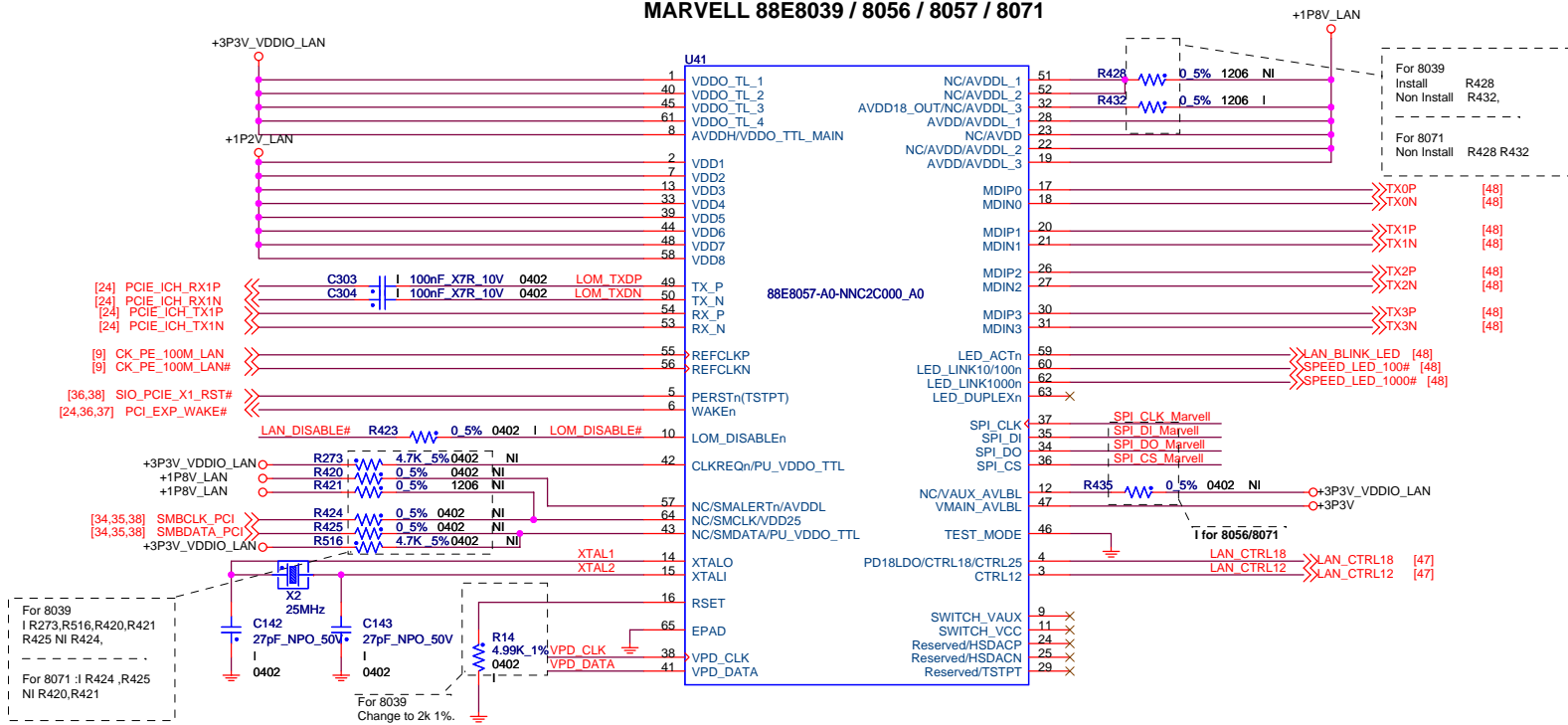


Color: White

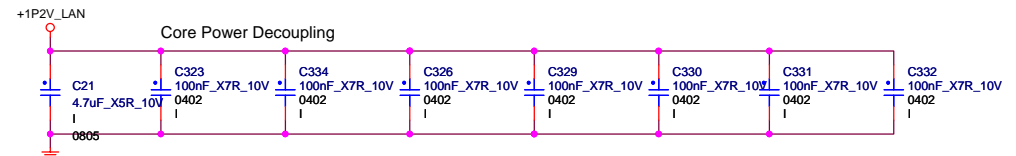
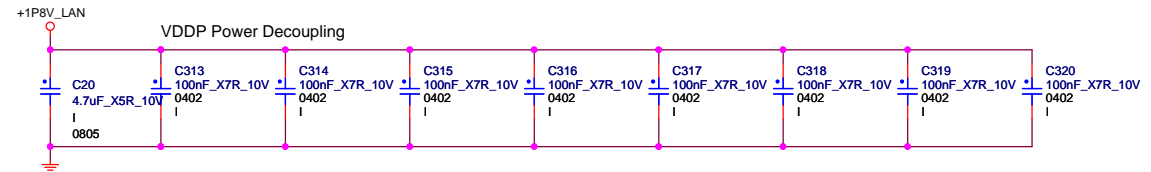
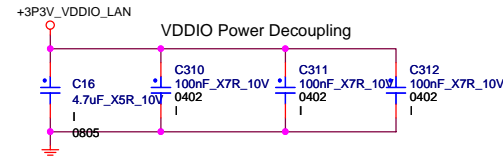
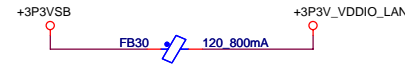
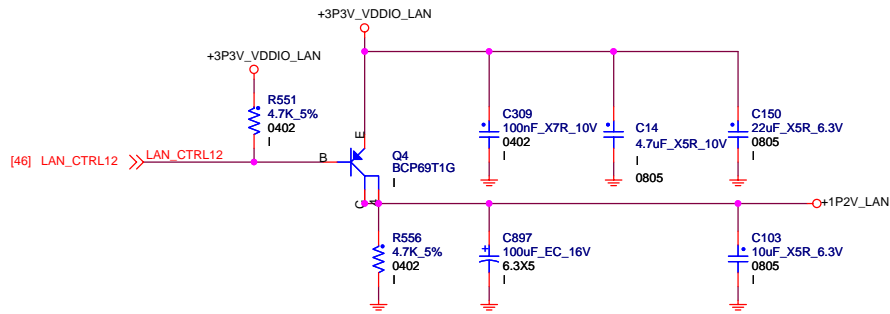
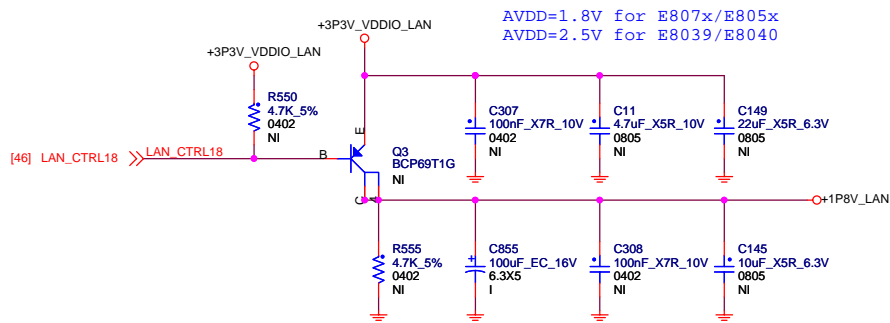


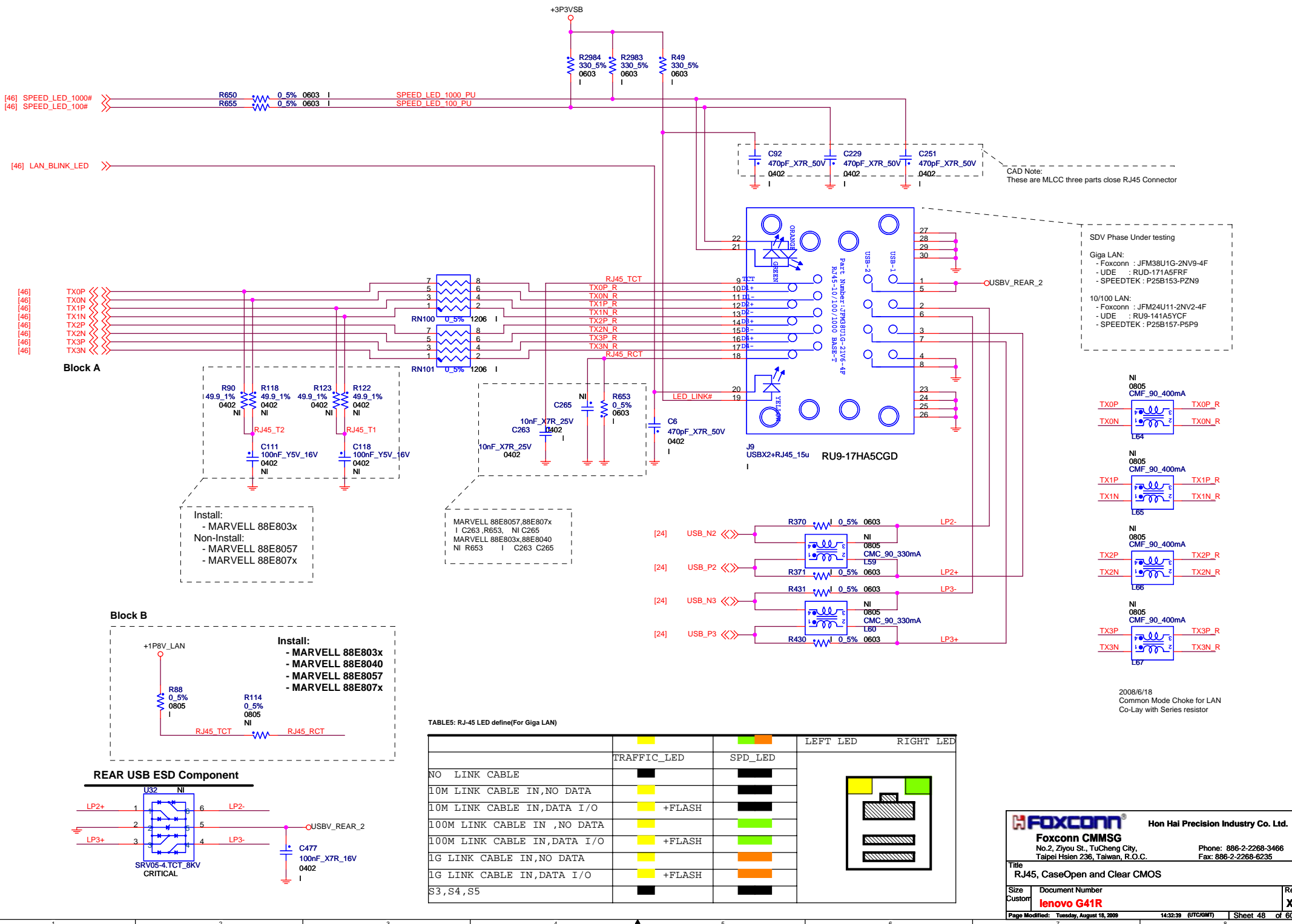
For EMI, add 2 .01uF Capacitors on +12V.

MARVELL 88E8039 / 8056 / 8057 / 8071



For 807x and ASF/DASH reserved.



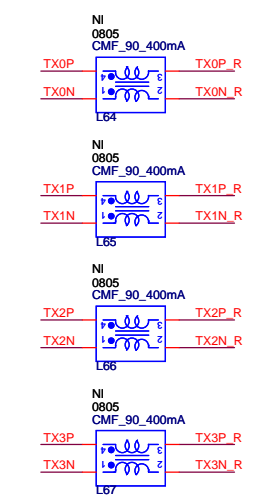


CAD Note:
These are MLCC three parts close RJ45 Connector

SDV Phase Under testing

Giga LAN:
- Foxconn : JFM38U1G-2NV9-4F
- UDE : RUD-171A5FRF
- SPEEDTEK : P25B153-PZN9

10/100 LAN:
- Foxconn : JFM24U11-2NV2-4F
- UDE : RU9-141A5YCF
- SPEEDTEK : P25B157-P5P9



2008/6/18
Common Mode Choke for LAN
Co-Lay with Series resistor

TABLE5: RJ-45 LED define(For Giga LAN)

	LEFT LED	RIGHT LED
	TRAFFIC_LED	SPD_LED
NO LINK CABLE		
10M LINK CABLE IN,NO DATA		
10M LINK CABLE IN,DATA I/O	+FLASH	
100M LINK CABLE IN ,NO DATA		
100M LINK CABLE IN,DATA I/O	+FLASH	
1G LINK CABLE IN,NO DATA		
1G LINK CABLE IN,DATA I/O	+FLASH	
S3,S4,S5		

Foxconn CMMSC
No.2, Ziyou St., TuCheng City,
Taipei Hsien 236, Taiwan, R.O.C.

Hon Hai Precision Industry Co. Ltd.
Phone: 886-2-2268-3466
Fax: 886-2-2268-6235

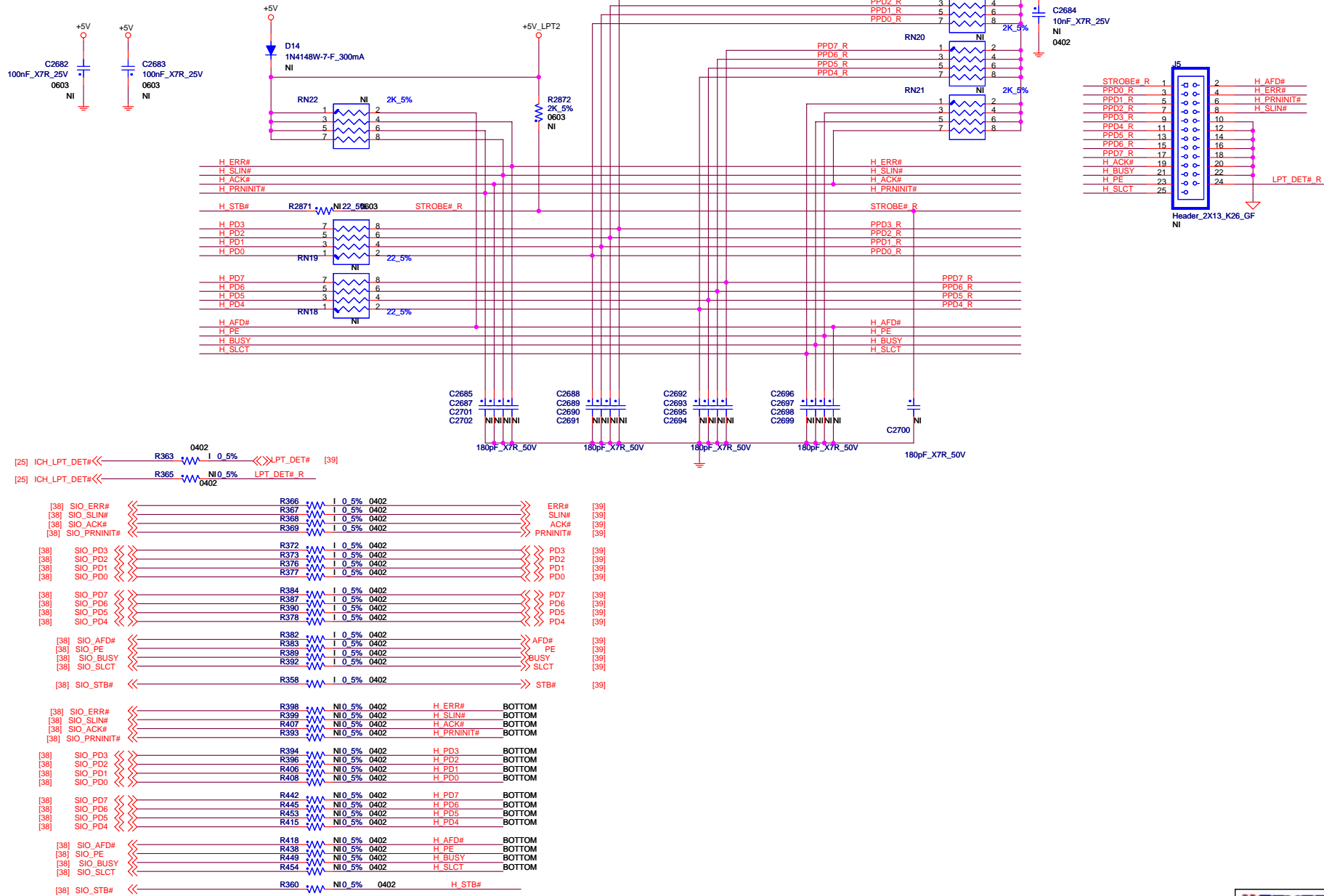
Title
RJ45, CaseOpen and Clear CMOS

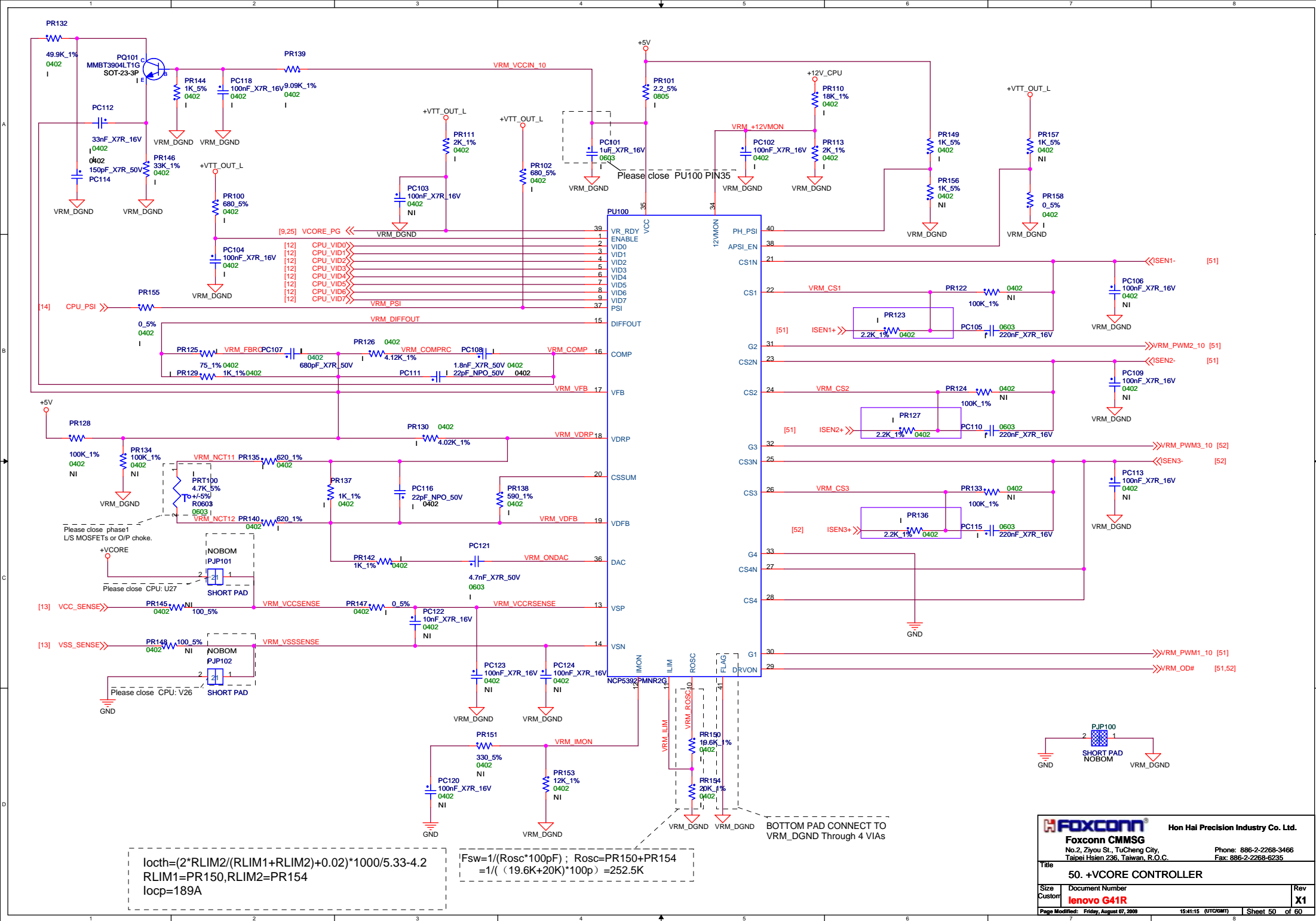
Size
Custom

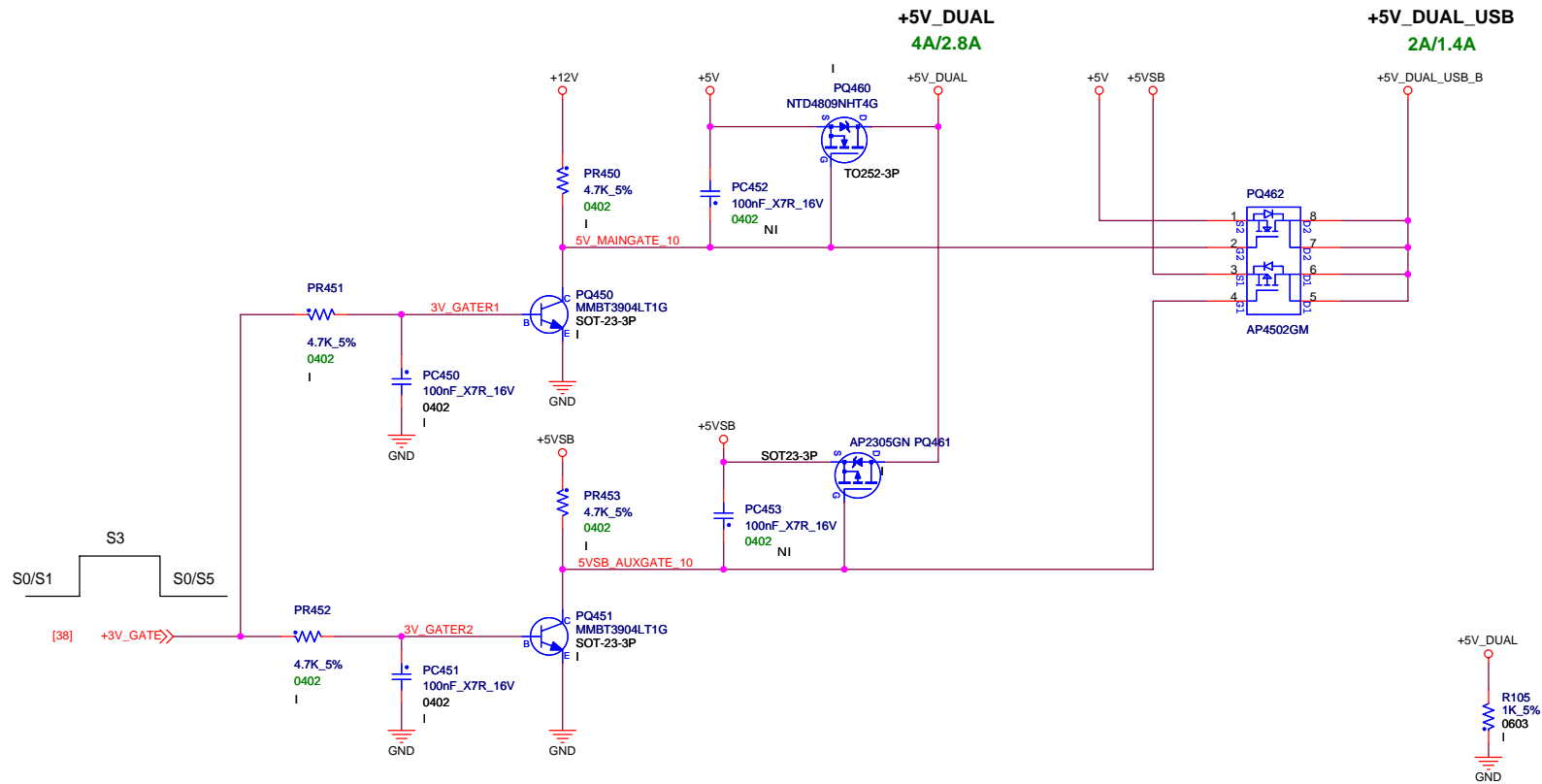
Document Number
lenovo G41R

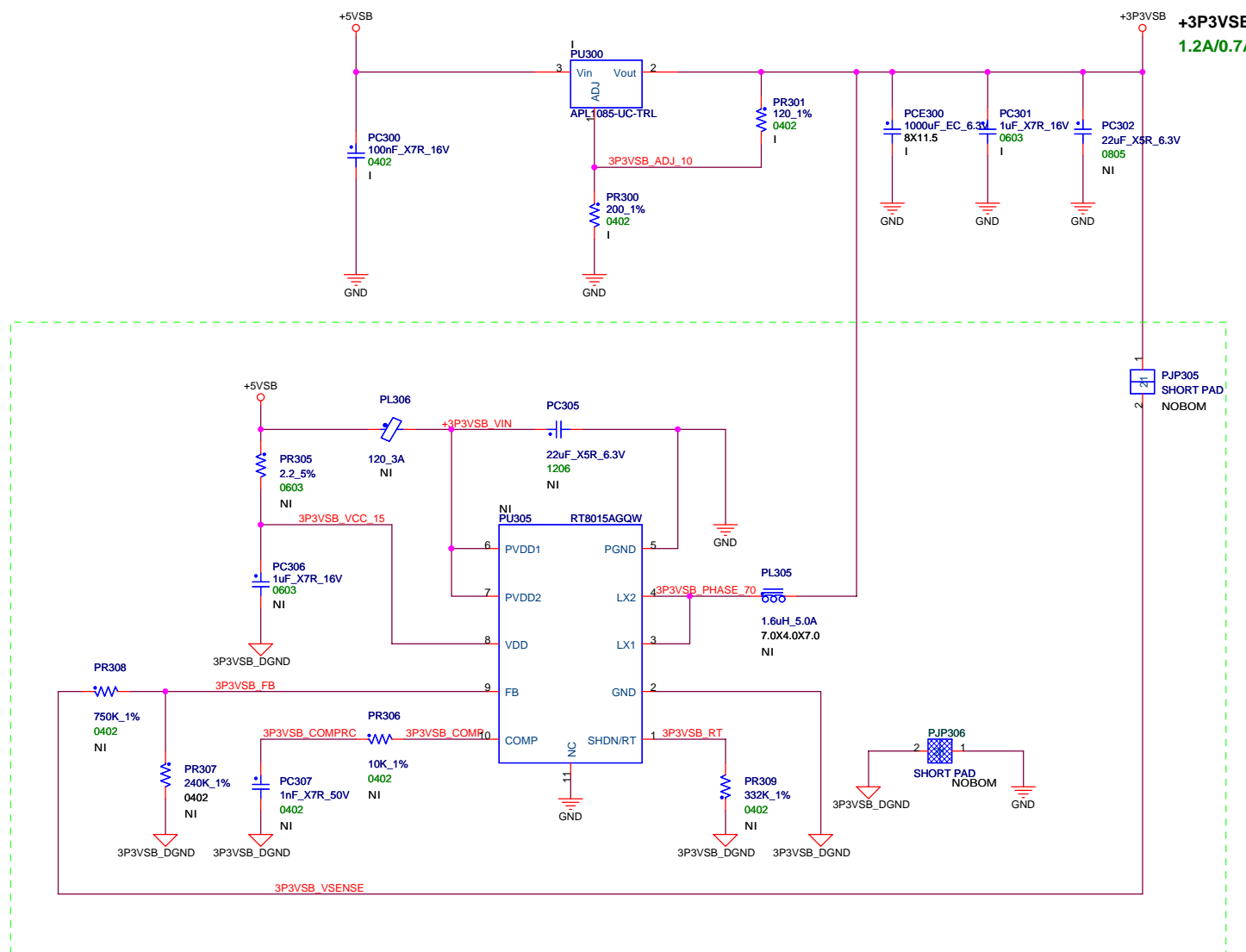
Rev
X1

Page Modified: Tuesday, August 18, 2009 14:32:39 (UTC+GMT) Sheet 48 of 60

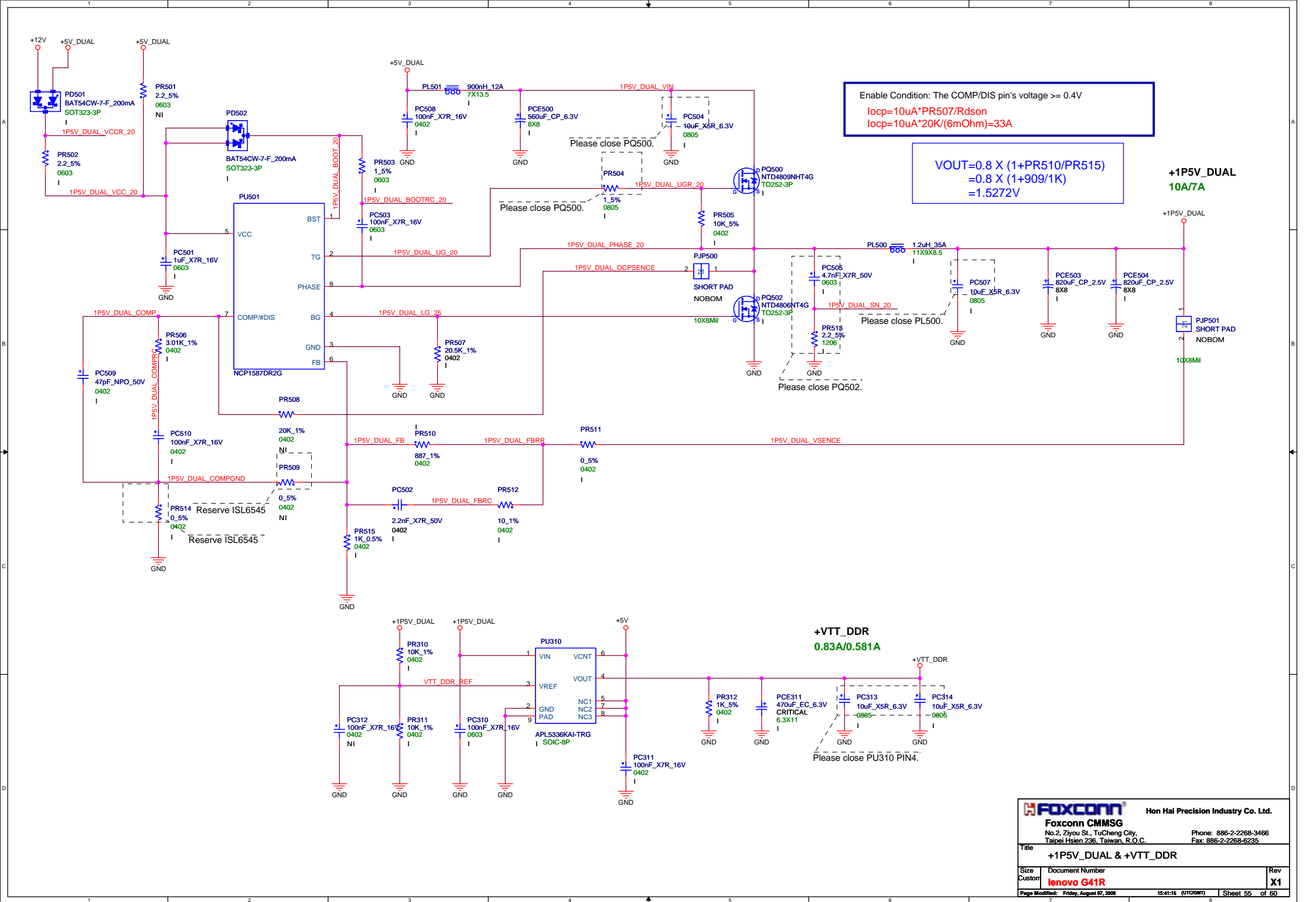


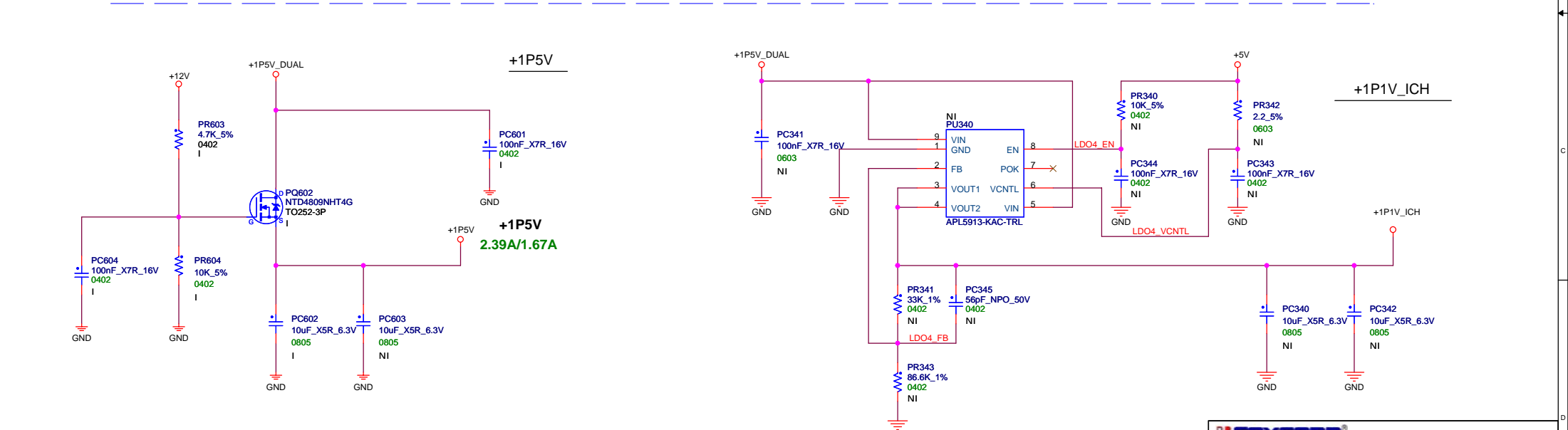
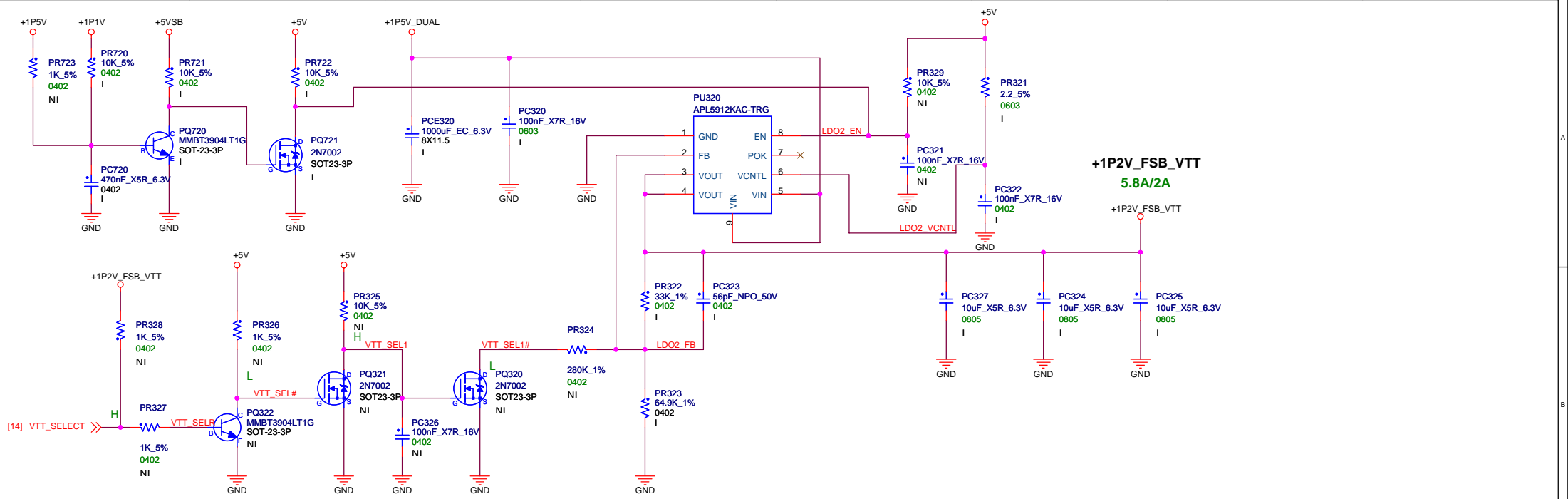






To reserve switch solution for energy star.





FOXCONN Foxconn CMMSG No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.		Hon Hai Precision Industry Co. Ltd. Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
Title +1P2V_FSB_VTT & +1P5V			
Size Custom	Document Number lenovo G41R		Rev X1
Page Modified: Friday, August 07, 2009		13:54:09 (UTC+08T)	Sheet 57 of 60

Name	Power Plane	Tolerance	Type	Default	Usage	Note
GPIO0 (Desktop Only)	Core	3.3V	I/O	GPIO	ICH_PECI_REQ#	N/A
GPIO1 REQ5#	Core	5V	I/O	GPIO	(Not used) ICH_P_REQ5#	Pull up 2.7K to 5V
GPIO2 PIRQE#	Core	5V	I/OD	GPIO	PCI_INT_E#	Pull up 8.2K to 3.3V.
GPIO3 PIRQF#	Core	5V	I/OD	GPIO	PCI_INT_F#	Pull up 8.2K to 3.3V.
GPIO4 PIRQG#	Core	5V	I/OD	GPIO	PCI_INT_G#	Pull up 8.2K to 3.3V.
GPIO5 PIRQH#	Core	5V	I/OD	GPIO	PCI_INT_H#	Pull up 8.2K to 3.3V.
GPIO6	Core	3.3V	I/O	GPIO	COMM_B_DETECT#	Pull up 8.2K to 3.3V
GPIO7	Core	3.3V	I/O	GPIO	(Not used) ICH_GP7	Pull up 8.2K to 3.3V
GPIO8	Resume	3.3V	I/O	GPIO	(Not used) ICH_GP8	Pull up 8.2K to 3.3VSB
GPIO9	Resume	3.3V	I/O	GPIO	(Not used) WOL_EN	Pull up 8.2K to 3.3VSB
GPIO10	Resume	3.3V	I/O	GPIO	SKTOCC#	Pull up 8.2K to 3.3VSB
GPIO11 SMBALERT#	Resume	3.3V	I/O	Native	(Not used) SMBALERT#	Pull up 10K to 3.3VSB
GPIO12	Resume	3.3V	I/O	GPIO	ICH_GP12 Green Power LED Control	None.
GPIO13	Resume	3.3V	I/O	GPIO	SIO_PME#	Pull up 1K to 3.3VSB
GPIO14	Resume	3.3V	I/O	GPIO	LPC_SMI#	Pull up 8.2K to 3.3VSB
GPIO15	Resume	3.3V	I/O	GPIO	CK_PCL_STOP# (Unstuffed)	Pull up 8.2K to 3.3VSB
GPIO16 (Desktop Only)	Core	3.3V	I/O	GPO	(Not Used)	Internal Pull-down 20K Test Point
GPIO17 GNT5#	Core	3.3V	I/O	GPO	ICH_GP17 Lenovo SPI write Protect	Pull down 1K to GND / Internal PU 20K BIOS memory range: SPI/PCI/LPC
GPIO18 (Desktop Only)	Core	3.3V	I/O	GPO	(Not Used)	None.
GPIO19 SATA1GP	Core	3.3V	I/O	GPIO	For Lenovo Thermal Sensor ID0	Pull up 8.2K to 3.3V.
GPIO20 (Desktop Only)	Core	3.3V	I/O	GPO	(Not Used) ICH_GP20	Pull up 8.2K to 3.3V.
GPIO21 SATA0GP	Core	3.3V	I/O	GPIO	TCM_DIS# TCM/TPM Header Disable. (Output)	Pull up 8.2K to 3.3V
GPIO22 REQ4#	Core	3.3V	I/O	Native	FRONT_USB_DET#_1	Pull up 8.2K to 3.3V
GPIO23 LDRQ1#	Core	3.3V	I/O	Native	(Not Used) ICH_GP23	Pull up 8.2K to 3.3V Internal PU 20K
GPIO24	Resume	3.3V	I/O	GPO	ICH_GP24 Yellow LED Control	None.
GPIO25	Resume	3.3V	I/O	GPO	CK_CPU_STOP#	Pull up 5.1K to 3.3VSB / Internal PU 20K DMI AC/DC Coupling Selection H: DC mode Low: AC mode
GPIO26	Resume	3.3V	I/O	GPO	(Not used) Testpoint ICH_GP26	None.
GPIO27	Resume	3.3V	I/O	GPO	Board ID0	Pull up 10K to 3.3VSB Pull down 2.7K to GND. (Reversed)
GPIO28	Resume	3.3V	I/O	GPO	Board ID2	Pull up 10K to 3.3VSB Pull down 2.7K to GND. (Reversed)
GPIO29 OC5#	Resume	3.3V	I/O	Native	USB_OC_FRONT1#	
GPIO30 OC6#	Resume	3.3V	I/O	Native	USB_OC_FRONT2#	
GPIO31 OC7#	Resume	3.3V	I/O	Native	USB_OC_FRONT2#	
GPIO32	Core	3.3V	I/O	GPO	LAN_DISABLE#	Pull up 1K to 3.3V Pull down 15K to GND
GPIO33	Core	3.3V	I/O	GPO	LPT_DET#	Pull up 8.2K to 3.3V

[illegible]

PCI Routing Table:			
PCI / PCI Express	Interrupt	Req / Gnt	ID SEL
PCI Slot1	EFGH	0	AD20
PCI Slot2	FGHE	2	AD26

Recommended values for variable GTLREF voltage divider		
GPIO60 / LINKALERT# CPU_GTLREF_CTRL_2	GPIO55 / GNT3# CPU_GTLREF_CTRL_1	Ratio Set
1	1	0.67
1	0	0.65
0	1	0.63
0	0	0.615

Thermal Informatio		
Thermal Sensor	Detect Method	Notes
CPU Temperature	PECI	
System Sensor	REMOTE1+/-	
CPU VR Sensor	REMOTE2 +/-	

PME / SMI Information	
Clock Information	

	Reg Offset (HEX)	TYPE	PCI RESET	VCC POR	SOFT RESET	VBAT POR	REGISTER	
ICH7	D31:F0 A4h							Bit0 - 0 system will return to S0 state - 1 sytem will return to the S5 state.
SCH5147	49 bit7=0							Bit[6,5] - 00 Power Supply Off - 01 Power Supply On - 10 Power Supply set to previous state, - 11 Power Supply Off.

Waiting

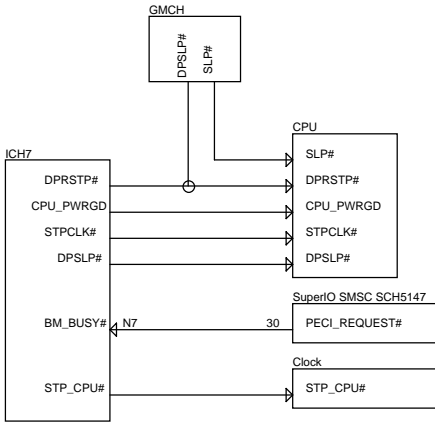
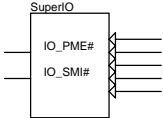
- BIOS Information:
- Device Address
 - PME/SMI Routing
 - Device Routing Information. (INIT,GNT,REQ.....)
 - Thermal Informatio (PECI, FAN.....)
 - GPIO Information. (SB,SIO,Audio.....)
 - Power Fail information as Lenovo Requirement


HW Straps Information:

BIOS Porting Consider:

- Clock:
- REF (14.318) need to Drive There device.
 - PCI need to Drive Two Device

Drives Three device. (REF)
1.Byte 9 point out internal bound pad number
2.Byte 13 point out internal I/O pad driver strength.
Therefore, we can understand, if you Byte 9 and Byte 13 to be "1", CV184 will support 3.5X loading.



		Hon Hai Precision Industry Co. Ltd.	
Foxconn CMMSG		No.2, Ziyou St., TuCheng City, Taipei Hsien 236, Taiwan, R.O.C.	
		Phone: 886-2-2268-3466 Fax: 886-2-2268-6235	
Title	BIOS Routing Information		
Size	Document Number		Rev
Custom	lenovo G41R		X1
Page Modified: Monday, June 15, 2009		19:45:46 (UTC+8MT)	Sheet 59 of 60